SPECIFICATION

BUFFER CONTROLLER

{FR101}

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1.0 SCOPE

This specification describes the Buffer Controller which serves as the data processing and/or master control element in a peripheral equipment and/or peripheral processing configuration.

Although the properties of the Buffer Controller are described in detail, an equally detailed description of their implementation in a peripheral environment, {Station}, is not within the scope of this specification.

2.0 APPLICABLE DOCUMENTS

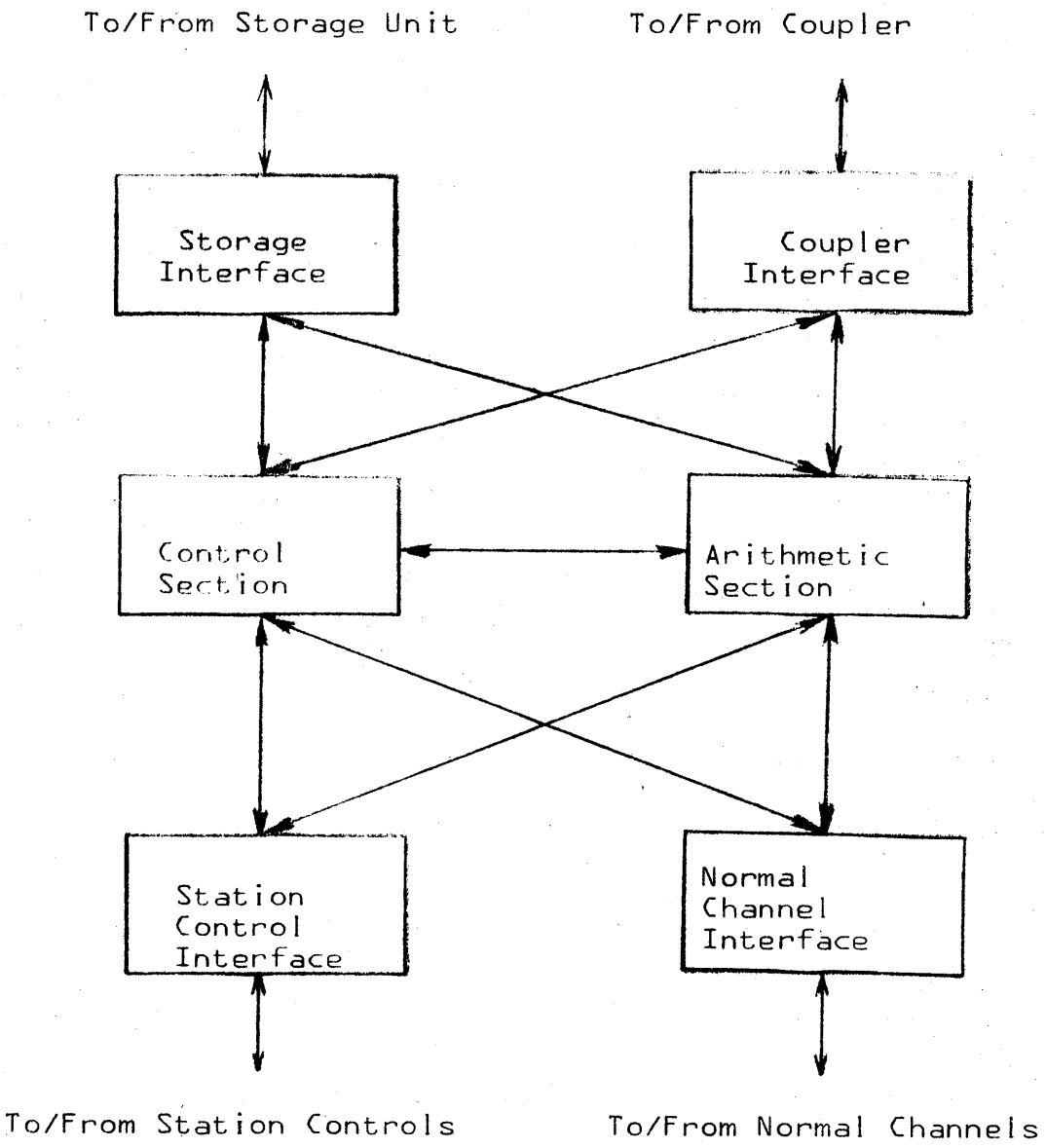
Engineering Standard 1.30.011
Engr. Spec. 20278200, High Speed 4096 word, 18-bit Memory
Engr. Spec. 52410700, Buffer Controller Normal Channels
Engr. Spec. 52410800, Buffer Controller Block Transfer Coupler
Engr. Spec. 11834700, TCS Gate - TOTO
Engr. Spec. 58018900, Buffer Controller Maintenance Console
Engr. Spec. 52319800, 1.1 u/s, 4096 word, 18 Bit Memory
Engr. Spec. 20277200, Three-layer Printed Circuit Board
Engr. Spec. 11828700, General Quality Spec. for ICs.
Engr. Spec. 11845900, Workmanship Spec. for CDC Mfg. ICs.
Engr. Spec. 52302000, Performance Spec for Connector Plates
CDC Spec. 10120300, General Quality Requirements

3.0 PERFORMANCE REQUIREMENTS

3.1 General Description

The Buffer Controller is an internally programmed, parallel mode, digital device intended to control a wide variety of peripheral devices. The Buffer Controller consists of six main sections as shown in the Block Diagram {Figure 1, page 9}.

In order to achieve its intended functions as a programmable device, the Buffer Controller {Equipment FR101} requires as a minimal addition, a Storage Unit which meets the interface requirements as described in Section 3.2.6. Although the Buffer Controller described by this Specification is actually a processor only, with a Storage Unit established as an absolute requirement, the term Buffer Controller is used in place of Buffer Controller Processor.



Buffer Controller Block Diagram

FIGURE 1

3.1.1 Control Section

The Control Section processes all instructions. In addition to sequencing arithmetic operations, this section issues timing and control signals to the Storage, Normal Channel, Coupler, and Station Control Interfaces.

The 16-bit Program Address Register is contained within this section and is referred to as the P Register throughout the remainder of this specification. The P Register is incremented within the Arithmetic section in 2's complement mode.

3.1.2 Arithmetic Section

The Arithmetic Section performs all arithmetic operations in 2's complement mode including those which form storage addresses. In addition to a 16-bit adder, this section contains the 16-bit Accumulator Register and two 16-bit Index Registers. These directly addressable registers are referred to as A, B1 and B2, respectively, throughout the remainder of this specification. All logical operations are performed within the Arithmetic Section.

The 16-bit adder includes a 17th output bit used to record the generation of a carry out of the adder during arithmetic operations involving the A Register. See section 3.2.3.2.

A parallel Shift Network provides the capability of right-shifting the contents of the A Register a maximum of 15 binary positions under the control of a 4-bit Shift Count. The Shift Network and Shift Count are referred to as SN and SC, respectively, throughout the remainder of this specification.

Note: Section 3.2 contains detailed information on the characteristics of both the Control and Arithmetic Sections.

1.1.3 Storage Interface

Although the Buffer Controller requires a Storage unit in order to achieve its intended functions as a programmable controller, Storage is treated as a separate equipment and is described in Engineering Specification 20278200.

Critical properties of the Storage unit which can be generally described as requirements at the Storage Interface of the Buffer Controller include:

200 n/s cycle, 90 n/s access times, {Optimum}.
18-bit read and write date interfaces
16-bit {maximum} address interface

Note: Throughout this specification, descriptions of the Storage Interface are based on a 200 n/s storage cycle time since the design of the Buffer Controller must be optimized for 200 n/s cycles.

Section 3.2.6 provides detailed information on the Storage Interface.

3.1.4 Normal Channel Interface

The Normal Channel Interface provides the Buffer Controller with the means for utilizing an input/output facility with programmable ▽Ready/Resume▽ controls. As a result, the Normal Channel Interface is oriented toward a one-for-one correspondence between Buffer Controller instructions and input/output transfers through the Normal Channel Interface. The general properties of this interface include the ability to uniquely select one of sixteen Normal Input Channels; and the ability to uniquely select one of sixteen Normal Output Channels for ▽ones▽ and/or ▽zeros▽ transfer. Normal Channel data transfers involve the A Register for 16-bit parallel operations or an instruction designated bit for ▽bit addressable▽ operations.

Section 3.2.7 provides detailed information on the Normal Channel Interface.

The description of DTL Normal Channels designed for attachment to the Buffer Controller Normal Channel Interface can be found in Engineering Specification 52410700.

3.1.5 Coupler Interface

The Coupler Interface provides the Buffer Controller with the means for utilizing an input/output facility with hardware "Ready/Resume" controls. As a result, I/O operations are oriented toward consecutive data transfers between the Buffer Controller and a Coupler via the Coupler Interface.

During Block Transfer Instructions the Buffer Controller references consecutive storage locations on the basis of external {Coupler} demands. The A Register is utilized for word count control and the transfer of data is terminated when the contents of the A Register become zero or upon the occurrence of an external terminate signal.

Section 3.2.8 provides detailed information on the Coupler Interface.

The description of a Coupler designed for attachment to the Buffer Controller Block Transfer Channel can be found in Engineering Specification 52410800.

3.1.6 Station Control Interface

The Station Control Interface provides facilities for controlling and monitoring Buffer Controller Operations. Certain input controls on this interface, such as "GO", "STOP", and "Master Clear", are required for basic operational control of the Buffer Controller. Other control inputs and status outputs on this interface, such as Breakpoint, Register Entry, Register Readout, Instruction Step, Timing Margins, etc., are facilities which may be externally exercised for hardware/software checkout and/or maintenance purposes.

Section 3.2.9 provides detailed information on the Station Control Interface.

3.2 Performance Characteristics

3.2.1 Instruction Formats

3.2.1.1 Instruction Format 1 {No Address}

00 04	05 07	08 11	12 15
f	a	s	t
5	3	4	4

f, function code
a, sub-function code
s, channel designator, instruction condition designator, or left-most 4 bits of an 8-bit immediate operand
t, bit designator, right-shift count, or right-most 4 bits of an 8-bit immediate operand

Format 1 instructions are considered to be No Address mode. No execution address is associated with these instructions since they perform control operations, contain an immediate operand, or perform operations involving only directly addressable registers.

The single exception to the preceding definition is the "LOAD from {A}" instruction in which the A Register initially contains the execution address. See section 3.2.5.24.

3.2.1.2 Instruction Format 2 {Single Address}

00 04	05	06 07	08 15
f	i	r	m
5	1	2	8

f, function code
i and r, addressing mode designators
m, base address

Addressing modes for Format 2 instructions are described with respect to the formation of an execution address, M. Parentheses are used to indicate "the contents of" a register or storage location. Where the right-most 8 bits of an instruction, m, are used directly or arithmetically to form a 16-bit address, zeros are appendended to m in the left-most bit positions, 00 through 07. All address arithmetic is performed 2's complement mode and does not alter the state of the Adder Generate Bit.

1.2.1.2.1 Direct Address; i = 0, r = 00_2

A direct address is formed by using only the right-most 8 bits of the instruction word. This addressing mode provides direct access to the first 256_{10} storage locations.

M = m

1.2.1.2.2 Index B1; i = 0, r = 01_2

An Index B1 modified address is formed by adding the contents of the B1 Register to the right-most 8 bits of the instruction word.

M = {B1} + m

1.2.1.2.3 Index B2; i = 0, r = 10_2

An Index B2 modified address is formed by adding the contents of the B2 Register to the right-most 8 bits of the instruction word.

M = {B2} + m

1.2.1.2.4 Relative Forward; i = 0, r = 11_2

A Relative Forward address is formed by adding the contents of the P Register to the right-most 8 bits of the instruction word.

M = {P} + m

1.2.1.2.5 Indirect Address; i = 1, r = 00_2

An Indirect address is formed by reading the contents of the storage location designated by the right-most 8 bits of the instruction word.

M = {m}

1.2.1.2.6 Indirect/Index B1; i = 1, r = 01_2

An Indirect/Index B1 modified address is formed by reading the contents of the storage location designated by the right-most 8 bits of the instruction word and adding the contents of the B1 Register.

M = {m} + {B1}

3.2.1.2.7 Indirect/Index B2; $i = 1, r = 10_2$

An Indirect/Index B2 modified address is formed by reading the contents of the storage location designated by the right-most 8 bits of the instruction word and adding the contents of the B2 Register.

$M = \{m\} + \{B2\}$

3.2.1.2.8 Relative Backward; $i = 1, r = 11_2$

A Relative Backward address is formed by subtracting the right-most 8 bits of the instruction word from the contents of the P Register.

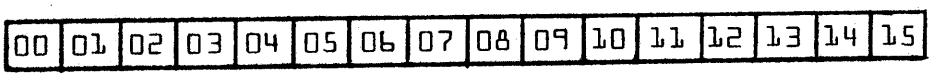
$M = \{P\} - m$

3.2.2 Data Formats

Data within the Storage and Arithmetic Sections of the Buffer Controller may be treated as 16-bit words or 8-bit bytes.

3.2.2.1 Word Format

Registers and Storage locations contain 16-bit words with the following bit designations:

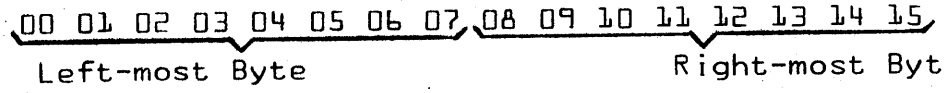


Bit 00 is the left-most bit. For signed quantities, the "one" state denotes a negative 2's complement quantity; the "zero" state denotes a positive quantity.

Bit 15 is the right-most bit.

3.2.2.2 Byte Format

Registers and Storage locations contain two 8-bit bytes within each 16-bit word with the following designations:



The left-most byte occupies the left-most bit positions, 00 through 07.

The right-most byte occupies the right-most bit positions, 08 through 15.

3.2.3 Internal Flags

3.2.3.1 Condition Bit

The Condition Bit is an internal flag that may be altered and sensed by program means. In the set or "one" state this flag is referred to as Condition True. In the clear or "zero" state this flag is referred to as Condition False. The following instructions are capable of altering the state of the Condition Bit:

Instruction	Page
Set Condition Equal: Internal Tests	24
Set Condition Equal: Bit t of Channel s	24
Test Index B1 No Address	29
Test Index B2 No Address	29
Test Index B1	31
Test Index B2	31
Input Block Transfer	35
Output Block Transfer	36

3.2.3.2 Adder Generate Bit

The Adder Generate Bit constitutes the 17th output bit of the adder and reflects the generation of an end-off carry following operand arithmetic for the following instructions:

Instruction	Page
Add No Address	28
Subtract No Address	28
Add	32
Subtract	32
Replace Add	33
Replace Add One	33

The Adder Generate Bit is not intended to convey any information concerning what is conventionally referred to as Arithmetic Overflow.

During multiple precision arithmetic operations the Adder Generate Bit provides an indication of Register Overflow by its presence when adding like-signed operands and by its absence when subtracting unlike-signed operands.

3.2.4 Instruction Tables

3.2.4.1 Format 1: Hexadecimal

Table 1 on page 18 provides the hexadecimal codes for the °f° and °a° portions of all Format 1 instructions. In addition, the °s° and °t° fields are designated by an X when used and by a 0 when unused. Explicit information with respect to these fields is contained within the detailed instruction descriptions in Section 3.2.5.

3.2.4.2 Format 2: Hexadecimal

Table 2 on page 19 provides the hexadecimal codes for the °f°, °i° and °r° portions of all Format 2 instructions. Designation of the address field, °m°, has been omitted from the table since its participation in address formation has been previously described in Section 3.2.1.2.

3.2.4.3 Instruction Execution Times

Table 3 on page 20 provides instruction execution times in number of storage reference cycles required for each instruction. The storage unit described in Engineering Specification 20278200 provides the Buffer Controller with a storage reference cycle of 200 n/s. ±.005%.

The following characteristics indicated by Table 3 deserve mention:

1. All Format 1 instructions require a single storage reference cycle with the exception of °Load from {A}°.

2. Indexing of an address does not impose a penalty on instruction execution time.

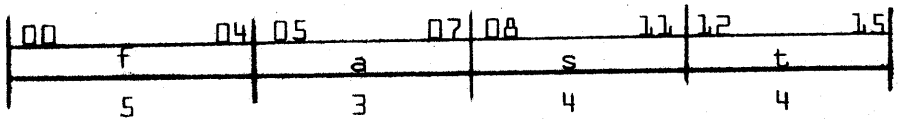
3. The execution time for Block Transfer instructions is dependent upon the number of transfers to be performed as well as the time required for each transfer.

   In Table 3: $k = n\{1+c\}$

   Where:
   - n = number of transfers,
   - 1 = one storage reference cycle,
   - c = a constant determined by the characteristics of the Coupler attached to the Block Transfer Channel.

4. Indirect Conditional Jumps require only a single storage reference cycle, {RNI}, when the jump condition is not satisfied.

Instruction Format 1:



INSTRUCTION DESCRIPTION	▿f▿ and ▿a▿ Fields	▿s▿ Field, ▿t▿ Field
Selective Stop	00	XX
Selective Set Bit t of A	01	0X
Selective Clear Bit t of A	02	0X
Selective Complement Bit t of A	03	0X
Count of Leading Zeroes in A_i to A_f	04	00
Shift A Right, t Places	05	XX
Transfer A to B1; {A} + ▿s▿ ▿t▿ → B1	06	XX
Transfer A to B2; {A} + ▿s▿ ▿t▿ → B2	07	XX
Set Condition Equal : Internal Tests	08	XX
Set Condition Equal : Bit t of Channel s	09	XX
Selective Set Bit t of Channel s	0A	XX
Selective Clear Bit t of Channel s	0B	XX
Input to A From Channel s	0C	X0
Set Channel s from A	0D	XX
Clear Channel s from A	0E	XX
Transfer A to Channel s	0F	XX
Add No Address	10	XX
Subtract No Address	11	XX
Exclusive or No Address	12	XX
Logical Product No Address	13	XX
Test Index B1 No Address	14	XX
Test Index B2 No Address	15	XX
Load A Complement No Address	16	XX
Load From {A}	17	XX

Table 1: Hexadecimal Codes for Format 1 Instructions

Instruction Format 2:

00 — 04	05	06 07	08 — 15
f	i	r	m
5	1	2	8

INSTRUCTION DESCRIPTION	Direct	Index B1	Index B2	Relative Forward	Indirect	Indirect/Index B1	Indirect/Index B2	Relative Backward
See Table 1	00 08	01 09	02 0A	03 0B	04 0C	05 0D	06 0E	07 0F
Enter A with Address	10 18	11 19	12 1A	13 1B	14 1C	15 1D	16 1E	17 1F
Enter B1 with Address Enter B2 with Address	20 28	21 29	22 2A	23 2B	24 2C	25 2D	26 2E	27 2F
Test Index B1 Test Index B2	30 38	31 39	32 3A	33 3B	34 3C	35 3D	36 3E	37 3F
Load A Load A Complement	40 48	41 49	42 4A	43 4B	44 4C	45 4D	46 4E	47 4F
Load Left-most Byte Load Right-most Byte	50 58	51 59	52 5A	53 5B	54 5C	55 5D	56 5E	57 5F
Add Subtract	60 68	61 69	62 6A	63 6B	64 6C	65 6D	66 6E	67 6F
Exclusive Or Logical Product	70 78	71 79	72 7A	73 7B	74 7C	75 7D	76 7E	77 7F
Replace Add Replace Add One	80 88	81 89	82 8A	83 8B	84 8C	85 8D	86 8E	87 8F
Replace Left-most Byte Replace Right-most Byte	90 98	91 99	92 9A	93 9B	94 9C	95 9D	96 9E	97 9F
Store Store Zeroes	A0 A8	A1 A9	A2 AA	A3 AB	A4 AC	A5 AD	A6 AE	A7 AF
Destructive Load Unconditional Jump	B0 B8	B1 B9	B2 BA	B3 BB	B4 BC	B5 BD	B6 BE	B7 BF
A Zero Jump A Nonzero Jump	C0 C8	C1 C9	C2 CA	C3 CB	C4 CC	C5 CD	C6 CE	C7 CF
A Positive Jump A Negative Jump	D0 D8	D1 D9	D2 DA	D3 DB	D4 DC	D5 DD	D6 DE	D7 DF
Condition True Jump Condition False Jump	E0 E8	E1 E9	E2 EA	E3 EB	E4 EC	E5 ED	E6 EE	E7 EF
Input Block Transfer Output Block Transfer	F0 F8	F1 F9	F2 FA	F3 FB	F4 FC	F5 FD	F6 FE	F7 FF

Table 2: Hexadecimal Codes for Format 2 Instructions

INSTRUCTION DESCRIPTION	Direct	Index B1	Index B2	Relative Forward	Indirect	Indirect/Index B1	Indirect/Index B2	Relative Backward
See Table 1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	2*
Enter A with Address	1	1	1	1	2	2	2	1
Enter B1 with Address	1	1	1	1	2	2	2	1
Enter B2 with Address	1	1	1	1	2	2	2	1
Test Index B1	2	2	2	2	3	3	3	2
Test Index B2	2	2	2	2	3	3	3	2
Load A	2	2	2	2	3	3	3	2
Load A Complement	2	2	2	2	3	3	3	2
Load Left-most Byte	2	2	2	2	3	3	3	2
Load Right-most Byte	2	2	2	2	3	3	3	2
Add	2	2	2	2	3	3	3	2
Subtract	2	2	2	2	3	3	3	2
Exclusive Or	2	2	2	2	3	3	3	2
Logical Product	2	2	2	2	3	3	3	2
Replace Add	3	3	3	3	4	4	4	3
Replace Add One	3	3	3	3	4	4	4	3
Replace Left-most Byte	3	3	3	3	4	4	4	3
Replace Right-most byte	3	3	3	3	4	4	4	3
Store	2	2	2	2	3	3	3	2
Store Zeroes	2	2	2	2	3	3	3	2
Destructive Load	3	3	3	3	4	4	4	3
Unconditional Jump	1	1	1	1	2	2	2	1
A Zero Jump	1	1	1	1	2**	2**	2**	1
A Nonzero Jump	1	1	1	1	2**	2**	2**	1
A Positive Jump	1	1	1	1	2**	2**	2**	1
A Negative Jump	1	1	1	1	2**	2**	2**	1
Condition True Jump	1	1	1	1	2**	2**	2**	1
Condition False Jump	1	1	1	1	2**	2**	2**	1
Input Block Transfer	1+k	1+k	1+k	1+k	2+k	2+k	2+k	1+k
Output Block Transfer	1+k	1+k	1+k	1+k	2+k	2+k	2+k	1+k

* Load from {A}
k is defined in 3.2.4.3
** Only 1 cycle is required for these instructions when the jump condition is not satisfied.

Table 3: Instruction Times in Number of Storage Reference Cycles

3.2.5 Instruction Descriptions

Each detailed instruction description begins with a heading that includes the instruction name and the associated hexadecimal code or range of codes.

The instruction descriptions make extensive use of abbreviations that have been previously defined in the preceding sections of this specification. In addition, the subscripts i and f are used to denote "initial" and "final", respectively, and refer to the contents of registers or storage locations.

Instructions which perform Input/Output are described to the extent that the Normal Channel and Coupler Interfaces may be meaningfully defined in sections 3.2.7 and 3.2.8, respectively. More precise information regarding Normal Channel and Coupler characteristics must be obtained from the appropriate Reference Documents listed in section 2.0.

Instructions which serve no purpose other than to increment the {P} by one are referred to as resulting in no operation.

Instruction words in which bit positions are unused, must have those bits in the zero state. Where unused bits in an instruction word are in the "one" state, the results of the instruction are undefined. As previously stated, each instruction heading provides the defined hexadecimal code or range of codes.

NOTE: In the case of the Selective Stop Instruction, {00XX} described in Section 3.2.5.1, since the "s" and "t" fields are unused to the extent that they do not participate in the execution of this instruction, they may be non-zero and are defined as having no effect. Subsequently these fields may be used in this instruction for identification, temporary storage or other program purposes.

3.2.5.1 | Selective Stop | 00 XX |

The execution of this instruction is dependent on the state of the ▽NOP-00▽ signal, a Selective Stop control input on the Station Control Interface defined in Section 3.2.9.

With the ▽NOP-00▽ signal equal to a ▽one▽ this instruction results in no operation.

With the ▽NOP-00▽ signal equal to a ▽zero▽ this instruction results in an immediate halt of program execution.

Once halted Buffer Controller program execution may be resumed, with the reading of the next instruction at P+1, through the use of additional control input facilities on the Station Control Interface. See section 3.2.9.

3.2.5.2 | Selective Set Bit t of A | 01 0X |

This instruction unconditionally sets bit t of A, where the 4-bit designator t specifies one of the sixteen bit positions in A. The remaining fifteen bits of A are left unchanged.

If bit t of A_i was already in the set state, then the instruction effectively results in no operation.

3.2.5.3 | Selective Clear Bit t of A | 02 0X |

This instruction unconditionally clears bit t of A, where the 4-bit designator t specifies one of the 16-bit positions in A. The remaining fifteen bits of A are left unchanged.

If bit t of A_i was already in the clear state, then the instruction effectively results in no operation.

3.2.5.4 | Selective Complement Bit t of A | 03 0X |

This instruction complements bit t of A, where the 4-bit designator t specifies one of the sixteen bit positions in A. The remaining fifteen bits of A are left unchanged.

The complement operation is performed so that: When bit t of A_i is set, bit t of A_f is clear; When bit t of A_i is clear, bit t of A_f is set.

3.2.5.5 | Count of Leading Zeroes in A_i to A_f | 04 00

This instruction scans the contents of A_i from left to right and transfers the count of leading zeroes into A_f as a 5-bit, right-justified quantity. The left-most 11 bits of A_f are cleared.

3.2.5.6 | Shift A Right, t Places | 05 0X and 058X

This instruction shifts the {A} right, t bit positions where t is a 4-bit shift count, SC.

The shift may be circular or end-off. When bit 08 of the instruction is a one, the shift is circular with right-most bits shifted end-around into left-most bit positions. When bit 08 of the instruction is a zero, the shift is end-off with zeroes inserted into left-most bit positions.

When t = 0 the instruction effectively results in no operation.

3.2.5.7 | Transfer A to B1; {A} + ▽s▽ ▽t▽ → B1 | 06 XX

This instruction adds the right-most 8 bits of the instruction word, with zeroes extended, to the {A} and transfers the sum to B1.

The state of the Adder Generate Bit is unaltered by the execution of this instruction.

3.2.5.8 | Transfer A to B2; {A} + ▽s▽ ▽t▽ → B2 | 07 XX

This instruction adds the right-most 8 bits of the instruction word, with zeroes extended, to the {A} and transfers the sum to B2.

The state of the Adder Generate Bit is unaltered by the execution of this instruction.

1.2.5.9 | Set Condition Equal: Internal Tests | 08 0X through 08 7X

This instruction forces the state of the Condition Bit to reflect the state of the selected internal test{s}.

When bit 09 of the instruction word is a one, the Condition Bit is forced True if the A Register contains an odd number of one bits, or

When bit 10 of the instruction word is a one, the Condition Bit is forced True if the Adder Generate Bit is a one, or

When bit 11 of the instruction word is a one, the Condition Bit is forced True if the right-most bit at the output of the Shift Network, SN15, is a one.

Since the {A} are statically enabled to the input of the Shift Network, the 4-bit Shift Count, t, determines the bit in A which is right shifted to emerge at SN15. The following table provides the hexadecimal values of t with the corresponding bit positions of A which are tested when bit 11 of the instruction word is a one.

t	A	t	A	t	A	t	A
0	15	4	11	8	07	C	03
1	14	5	10	9	06	D	02
2	13	6	09	A	05	E	01
3	12	7	08	B	04	F	00

Since the selected internal tests will force the Condition Bit True on an "inclusive or" basis, all of the selected tests must be zero in order to force the Condition Bit False. Likewise, if bits 09, 10 and 11 of the instruction word are zeroes, the Condition Bit is forced False.

3.2.5.10 | Set Condition Equal: Bit t, Channel s | 09 XX

This instruction forces the state of the Condition Bit to reflect the state of the selected bit on the selected Normal Input Channel.

Force the Condition Bit True if bit t of Normal Input Channel s is a one; Force the Condition Bit False if bit t of Normal Input Channel s is a zero.

The 4-bit designator s specifies one of sixteen possible Normal Input Channels and the 4-bit designator t specifies one of the sixteen-bit positions to be tested within that channel. If the designated Input Channel is not physically present, the Condition Bit is forced True.

3.2.5.11 | Selective Set Bit t of Channel s | 0A XX |

This instruction unconditionally sets bit t of Normal Output Channel s.

The 4-bit designator s specifies one of sixteen possible Normal Output Channels and the 4-bit designator t specifies one of the sixteen bit positions to be set within that channel. The remaining fifteen bits of the channel are left unchanged.

If bit t of channel s was initially in the set state or if Normal Output Channel s is not physically present, the instruction effectively results in no operation.

3.2.5.12 | Selective Clear Bit t of Channel s | 0B XX |

This instruction unconditionally clears bit t of Normal Output Channel s.

The 4-bit designator s specifies one of sixteen possible Normal Output Channels and the 4-bit designator t specifies one of the sixteen bit positions to be cleared within that channel.

If bit t of channel s was initially in the clear state or if Normal Output Channel s is not physically present, the instruction effectively results in no operation.

3.2.5.13 | Input To A From Channel s | 0C X0

This instruction transfers a word from Normal Input Channel s to A.

The 4-bit designator s specifies one of sixteen possible Normal Input Channels.

If Normal Input Channel s is not physically present, {Af} will consist of all ones; $FFFF_{16}$.

3.2.5.14 | Set Channel s From A | 0D X0 or 0D X8

This instruction sets bits on Normal Output Channel s according to the {A}.

When bit 12 of the instruction word is a zero, this instruction sets bits on Normal Output Channel s where corresponding ones are present in A. Where zeros are present in A, corresponding bits on the Normal Output Channel are left unchanged.

When Bit 12 of the instruction word is a one, this instruction sets bits on Normal Output Channel s where corresponding zeros are present in A. Where ones are present in A, corresponding bits on the Normal Output Channel are left unchanged.

The 4-bit designator s specifies one of sixteen possible Normal Output Channels.

If Normal Output Channel s is not physically present, the instruction results in no operation.

1.2.5.15 | Clear Channel s From A | OE X0 or OE X8

This instruction clears bits on Normal Output Channel s according to {A}.

When bit 12 of the instruction word is a zero, this instruction clears bits on Normal Output Channel s where corresponding zeros are present in A. Where ones are present in A, corresponding bits on the Normal Output Channel are left unchanged.

When bit 12 of the instruction word is a one, this instruction clears bits on Normal Output Channel s where corresponding ones are present in A. Where zeros are present in A, corresponding bits on the Normal Channel are left unchanged.

The 4-bit designator s specifies one of sixteen possible Normal Output Channels.

If Normal Output Channel s is not physically present, the instruction results in no operation.

3.2.5.16 | Transfer A to Channel s | OF X0 or OF X8

This instruction transfers the {A} directly or in one's complement mode to Normal Output Channel s.

When bit 12 of the instruction word is a zero, this instruction force transfers the {A} directly to Normal Output Channel s.

When bit 12 of the instruction word is a one, this instruction force transfers the one's complement of {A} to Normal Output Channel s.

The 4-bit designator s specifies one of sixteen possible Normal Output Channels.

If Normal Output Channel s is not physically present, the instruction results in no operation.

3.2.5.17 | Add No Address | 10 XX

This instruction adds the right-most 8 bits of the instruction word, with zeroes extended, to the $\{A\}_i$ and transfers the sum to A_f.

The Adder Generate bit receives the end-off carry from the adder at the time the result is transferred to A.

3.2.5.18 | Subtract No Address | 11 XX

This instruction subtracts the right-most 8 bits of the instruction word, with zeroes extended, from the $\{A\}_i$ and transfers the difference to A_f.

The Adder Generate bit receives the end-off carry from the adder at the time the result is transferred to A.

3.2.5.19 | Exclusive Or No Address | 12 XX

This instruction performs an exclusive or with the right-most 8 bits of the instruction word and the right-most 8 bits of A_i and places the result in A_f. The left-most 8 bits of A_i remain unchanged.

The exclusive or operation is performed for the following truth table:

Bit n of A_i	Bit n of the Immediate Operand	Bit n of A_f
0	0	0
0	1	1
1	0	1
1	1	0

n = 08 through 15

3.2.5.20 | Logical Product No Address | 13 XX

This instruction performs the logical product with the right-most 8 bits of the instruction word and the right-most 8-bits of A_i and places the result in A_f. The left-most 8 bits of A_f are cleared.

The logical product operation is performed for the following truth table:

Bit n of A_i	Bit n of the Immediate Operand	Bit n of A_f
0	0	0
0	1	0
1	0	0
1	1	1

n = 08 through 15

3.2.5.21 | Test Index B1 No Address | 14 XX

This instruction compares the right-most 8 bits of the instruction word with the right-most 8 bits initially contained in B1.

If the quantities are equal, the Condition Bit is forced True and the $\{B1\}_i$ are left unchanged.

If the quantities are not equal, the Condition Bit is forced False and the $\{B1\}_i$ are increased by one; $\{B1\}_i + 1 \rightarrow B1_f$.

3.2.5.22 | Test Index B2 No Address | 15 XX

This instruction compares the right-most 8 bits of the instruction word with the right-most 8 bits initially contained in B2.

If the quantities are equal, the Condition Bit is forced True and the $\{B2\}_i$ are left unchanged.

If the quantities are not equal, the Condition Bit is forced False and the $\{B2\}_i$ are increased by one; $\{B2\}_i + 1 \rightarrow B2_f$.

3.2.5.23 | Load A Complement No Address | 16 XX

This instruction performs the 2's complement of the right-most 8 bits of the instruction word, with zeroes extended, and transfers the result to A.

3.2.5.24 | Load From {A}; $\{\{A_i\} + {}^{\nabla}s^{\nabla}\ {}^{\nabla}t^{\nabla}\} \rightarrow A_f$ | 17 XX

This instruction transfers the {M} to A.

The execution address, M, is formed by adding the right-most 8 bits of the instruction word to the $\{A\}_i$.

3.2.5.25 | Enter A With Address | 18 XX through 1FXX

This instruction transfers M to A.

As a result of using the execution address as an operand, four variations of this instruction become noteworthy:

When M = m, the instruction performs what is conventionally described as Enter A.

When M = {B1} + m and m = 00, the instruction performs an inter-register transfer from B1 to A.

When M = {B2} + m and m = 00, the instruction performs an inter-register transfer from B2 to A.

When M = {P} ± m and m = 00, the instruction performs an inter-register transfer from P to A.

1.2.5.26 | Enter B1 With Address | 20 XX through 27 XX

This instruction transfers M to B1.

As a result of using the execution address as an operand, six variations of this instruction become noteworthy:

When M = m, the instruction performs what is conventionally described as Enter Index.

When M = {B1} + m, the instruction performs what is conventionally described as Increase Index.

When M = {B2} + m and m = 00, the instruction performs an inter-register transfer from B2 to B1.

When M = {P} ± m and m = 00, the instruction performs an inter-register transfer from P to B1.

When M = {m}, the instruction performs what is conventionally described as Load Index.

When M = {B1} + {m}, the instruction performs an Add to Index operation.

1.2.5.27 | Enter B2 With Address | 28 XX through 2F XX

This instruction transfers M to B2.

As a result of using the execution address as an operand, six variations of this instruction become noteworthy:

When M = m, the instruction performs what is conventionally described as Enter Index.

When M = {B2} + m, the instruction performs what is conventionally described as Increase Index.

When M = {B1} + m and m = 00, the instruction performs an inter-register transfer from B1 to B2.

When M = {P} ± m and m = 00, the instruction performs an inter-register transfer from P to B2.

When M = {m}, the instruction performs what is conventionally described as Load Index.

When M = {B2} + {m}, the instruction performs an Add to Index operation.

1.2.5.28 | Test Index B1 | 30 XX through 37 XX

This instruction compares the {M} to the $\{B1\}_i$.

If the quantities are equal, the Condition Bit is forced True and the $\{B1\}_i$ are left unchanged.

If the quantities are not equal, the Condition Bit is forced False and the $\{B1\}_i$ are increased by one; $\{B1\}_i + 1 \rightarrow B1_f$.

1.2.5.29 | Test Index B2 | 38 XX through 3F XX

This instruction compares the {M} to the $\{B2\}_i$.

If the quantities are equal, the Condition Bit is forced True and the $\{B2\}_i$ are left unchanged.

If the quantities are not equal, the Condition Bit is forced False and the $\{B2\}_i$ are increased by one; $\{B2\}_i + 1 \rightarrow B2_f$.

1.2.5.30 | Load A | 40 XX through 47 XX

This instruction transfers the {M} to A.

1.2.5.31 | Load A Complement | 48 XX through 4F XX

This instruction transfers the 2's complement of the {M} to A.

Although taking the 2's complement of the quantities 0000 and 8000_{16} leaves the numbers unaltered, the hardware does not detect them as exceptions.

1.2.5.32 | Load Left-most Byte | 50 XX through 57 XX

This instruction transfers the left-most byte from the execution address M to the right-most byte position of A.

The left-most byte position of A_f is cleared.

1.2.5.33 | Load Right-most Byte | 58 XX through 5F XX

This instruction transfers the right-most byte from the execution address M to the right-most byte position of A.

The left-most byte position of A_f is cleared.

1.2.5.34

Add	60 XX through 67 XX

This instruction adds {M} to $\{A\}_i$ and transfers the sum to A_f.

The Adder Generate Bit receives the end-off carry from adder at the time the result is transferred to A_f.

1.2.5.35

Subtract	68 XX through 6F XX

This instruction subtracts the {M} from the $\{A\}_i$ and transfers the difference to A_f.

The Adder Generate bit receives the end-off carry from the adder at the time the result is transferred to A_f.

1.2.5.36

Exclusive Or	70 XX through 77 XX

This instruction performs an exclusive or with the {M} and $\{A\}_i$ and transfers the result to A_f.

The exclusive or operation is performed for the following truth table:

Bit n of $\overline{A_i}$	Bit n of the Storage Operand	Bit n of A_f
0	0	0
0	1	1
1	0	1
1	1	0

n = 00 through 15

1.2.5.37

Logical Product	78 XX through 7F XX

This instruction performs a logical product with the {M} and the $\{A\}_i$ and transfers the result to A_f.

The logical product operation is performed for the following truth table:

Bit n of A_i	Bit n of the Storage Operand	Bit n of A_f
0	0	0
0	1	0
1	0	0
1	1	1

n= 00 through 15

3.2.5.38 | Replace Add | 80 XX through 87 XX

This instruction adds the $\{M\}_i$ to the $\{A\}_i$ and transfers the sum to A_f. The $\{A\}_f$ are then stored at M.

The Adder Generate bit receives the end-off carry from the adder at the time the sum is transferred to A_f.

3.2.5.39 | Replace Add One | 88 XX through 8F XX

This instruction adds one to the $\{M\}_i$ and transfers the sum to A_f. The $\{A\}_f$ are then stored at M.

The Adder Generate bit receives the end-off carry from the adder at the time the sum is transferred to A.

3.2.5.40 | Replace Left-most Byte | 90 XX through 97 XX

This instruction stores the right-most byte of A_i into the left-most byte position at M. The right-most byte at M is left unchanged and the $\{A\}_f = \{M\}_f$.

3.2.5.41 | Replace Right-most Byte | 98 XX through 9F XX

This instruction stores the right-most byte of A_i into the right-most byte position at M. The left-most byte at M is left unchanged and the $\{A\}_f = \{M\}_f$.

3.2.5.42 | Store | A0 XX through A7 XX

This instruction stores {A} at M.

3.2.5.43 | Store Zeroes | A8 XX through AF XX

This instruction stores zeroes at M.

3.2.5.44 | Destructive Load | B0 XX through B7 XX

This instruction transfers the $\{M\}_i$ to A_f and stores zeroes at M.

1.2.5.45 Jump Instructions

Only jump instructions are capable of using execution address M as the address of the next instruction. The exercise of this capability is referred to as a jump exit.

Unless a jump exit is specified, all instructions perform a normal exit in which the address of the next instruction is formed by adding one to the address of the current instruction. Conditional jump instructions for which the jump conditions are not met, perform a normal exit.

3.2.5.45.1

Unconditional Jump	B8 XX through BF XX

This instruction unconditionally performs a jump exit.

3.2.5.45.2

A Zero Jump	C0 XX through C7 XX

This instruction performs a jump exit if the {A} consists entirely of zeroes.

3.2.5.45.3

A Nonzero Jump	C8 XX through CF XX

This instruction performs a jump exit if the {A} does not consist entirely of zeroes.

3.2.5.4

A Positive Jump	D0 XX through D7 XX

This instruction performs a jump exit if the {A} consists of a positively signed quantity.

3.2.5.45.5

A Negative Jump	D8 XX through DF XX

This instruction performs a jump exit if the {A} consists of a negatively signed quantity.

3.2.5.45.6

Condition True Jump	E0 XX through E7 XX

This instruction performs a jump exit if the Condition Bit is True.

3.2.5.45.7

Condition False Jump	E8 XX through EF XX

This instruction performs a jump exit if the Condition Bit is False.

	Input Block Transfer	F0 XX through F7 XX

This instruction transfers data from the Coupler Interface into Buffer Controller Storage beginning at the execution address, M. This instruction requires that the $\{A\}_i$ be equal to the 2's complement of the number of words to be transferred.

Initiation: When the "Ready" signal on the Coupler Interface is a zero at the time this instruction is read from storage, the Condition Bit is forced False and the instruction performs an immediate normal exit with the $\{A\}_i$ left unchanged. When the "Ready" signal on the Coupler Interface is a one at the time this instruction is read from Storage, the execution address, M, is formed and transferred to the Storage Address Register, S. See section 3.2.8.2.1 for a description of the "Ready" signal.

Transfer: At the time each input word is supplied to the Coupler Interface, a storage reference cycle is performed to store the word at the address contained in S, to increase the {A} by one, and to increase the {S} by one.

Termination: The instruction terminates the input transfer, performs a normal exit, and forces the Condition Bit True when increasing the {A} by one results in the {A} becoming equal to zero. The instruction terminates the input transfer, performs a normal exit and forces the Condition Bit False when a "Terminate" signal is received on the Coupler Interface. See Section 3.2.8.2.3.

Notes: If the $\{A\}_i$ are equal to zero, the number of words to be transferred is translated as $65,536_{10}$.

When execution of this instruction leaves the Condition Bit True, it indicates that the "Ready" signal was initially a one and that the designated number of input words was transferred to Buffer Controller Storage.

When execution of this instruction leaves the Condition Bit False, it indicates that the "Ready" signal was initially a zero or that a "Terminate" signal was received on the Coupler Interface. The $\{A\}_f$ may be interpreted in order to determine the number of words, if any, transferred to Buffer Controller Storage.

3.2.5.47 | Output Block Transfer | F8 XX through FF XX

Beginning at execution address, M, this instruction transfers data from Buffer Controller Storage to the Coupler Interface. This instruction requires that the $\{A\}_i$ be equal to the 2's complement of the number of words to be transferred.

Initiation: When the ▽Ready▽ signal on the Coupler Interface is a zero at the time this instruction is read from storage, the Condition Bit is forced False and the instruction performs an immediate normal exit with the $\{A\}_i$ left unchanged. When the ▽Ready▽ signal on the Coupler Interface is a one at the time this instruction is read from storage, the execution address, M, is formed and transferred to the Storage Address Register, S.

Transfer: A storage reference cycle is performed to read each output word from the address contained in S, increase the {A} by one and increase the {S} by one. Each output word is present on the Coupler Interface until accepted {▽Reply▽} or rejected {▽Terminate▽} according to the description of Control Signals in Section 3.2.8.

Termination: This instruction terminates the output transfer, performs a normal exit, and forces the Condition Bit True at the time the last output word, {A} = zero, is accepted on the Coupler Interface. This instruction terminates the out put transfer, performs a normal exit, and forces the Condition Bit False at the time an output word is rejected by a ▽Terminate▽ signal on the Coupler Interface.

Notes: If the $\{A\}_i$ are equal to zero, the number of words to be transferred is interpreted as $65,536_{10}$.

When execution of this instruction leaves the Condition Bit True, it indicates that the Ready Signal was initially a one and that the designated number of output words were transferred from Buffer Controller Storage and accepted at the Coupler Interface.

When execution of this instruction leaves the Condition Bit False, it inidicates that the Ready Signal was initially a zero or that a ▽Terminate▽ signal was received on the Coupler Interface. The $\{A\}_f$ may be interpreted in order to determine the number of words transferred from Buffer Controller Storage to the Coupler Interface.

1.2.6 Storage Interface

The Storage Interface is defined as the 55 unique signals that link the Buffer Controller Control Section to its Storage Section. These signals are implemented using the TCS differential transmission scheme described in Engineering Specification 11834700, Section 6.10.2. They are functionally grouped into the three major categories of Control, Address and Data.

1.2.6.1 Storage Control Signals

Two storage control signals are generated by the Control Section and consist of an Access Command and a Write Command. A third control signal, Master Clear, is also available from the Control Section to the Storage Interface.

Note: The Buffer Controller requires that the Storage Unit be self-timed for all operations internal to itself.

1.2.6.1.1 Access Command

The access command is a 15 to 25 n/s pulse which initiates the storage reference cycle. The minimum time from the leading edge of one access command pulse to the leading edge of the next access command pulse is 200 n/s. See Figures 2a and 2b, page 40.

1.2.6.1.2 Write Command

The write command is a control signal that is stable at the leading edge of the access command and remains unchanged for a minimum of 175 n/s thereafter. The "one" state of this signal commands the storage section to write new information at the selected storage location. The "zero" state of this signal commands the storage section to read information from the selected storage location. See Figures 2a and 2b, page 40.

1.2.6.1.3 Master Clear

The Master Clear signal is not originated by the Buffer Controller but is received on the Station Control Interface and repeated by the Control Section for transmission to the Storage Unit. {See Section 3.2.9 for a description of the Master Clear inputs to the Buffer Controller.}

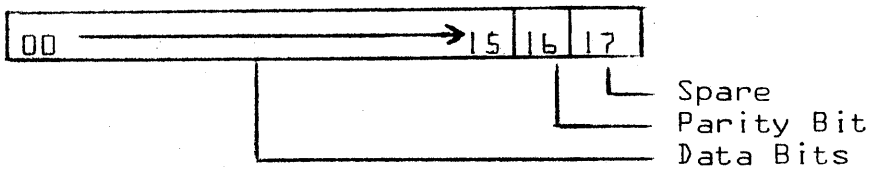
1.2.6.2 Storage Address

The sixteen address lines provided at the Storage Interface are stable at the leading edge of the access command and remain unchanged for a minimum of 175 n/s thereafter. These address lines determine which storage word is selected from a maximum of $65,536_{10}$. See Figures 2a and 2b, Page 40.

1.2.6.3 Storage Data

Eighteen data lines are available for transmission of information read from storage and 18 data lines are available for transmission of information written into storage.

With respect to the Storage Section, each word consists of 18 bits with no special significance attached to the position of bits within each word. However, Read and Write Data line bit positions must appropriately correspond. With respect to the Control Section of the Buffer Controller, the 18 bits within each storage word are designated as follows:



1.2.6.3.1 Read Data Lines

The 18 lines associated with information read from storage are referred to as read data lines. During storage references in which the write command is a "zero", these lines become stable a maximum of 90 n/s after the leading edge of the access command and remain stable for a minimum of 60 n/s thereafter. See Figure 2a, page 40.

1.2.6.3.2 Write Data Lines

The 18 lines associated with information to be written into storage are referred to as write data lines. During storage references in which the write command is a "one", the write data lines supply stable levels to the Storage Section a maximum of 25 n/s after the leading edge of the access command and remain stable for a minimum of 175 n/s thereafter. See Figure 2b on page 40.

1.1.6.4 Special Storage Controls

In addition to the 55 signals previously defined for the Storage Interface, the following 6 signals are required to facilitate the implementation of Storage Units with cycle times in the range of .2u/s to 1.1u/s.

These six signals are implemented using the TCS single-ended transmission scheme described in Engineering Specification 11834700, Section 10.6.1.

3.2.6.4.1 Crystal Input and Feedback Controls

Two signals are required to interface the Buffer Controller with a crystal whose frequency is a function of the cycle/access time of the Storage Unit. Since the crystal amplifier and count down logic are located within the Control Section of the Buffer Controller the crystal connections on the Storage Interface consist of an input signal and a feedback signal.

The crystal for which these connections are intended is a 32 pfd, .005% frequency tolerance crystal in the 20Mz to 3.6Mz range.

Crystal frequency, F, is related to storage times according to the following:

1/(F/4) = Storage cycle
1/(F/2) = Storage access + 10n/s

3.2.6.4.2 End of Access/Cycle Input Controls

In response to each Access Command, the Storage Unit must provide two 15 to 25 n/s pulses at separate input terminals to the Storage Interface. The first of these pulses must occur at the end of access time. The second pulse must occur at the end of cycle time.

3.2.6.4.3 End of Access/Cycle Output Controls

Following each Access Command the Buffer Controller generates two 15 to 25 n/s pulses at separate output terminals on the Storage Interface. The first of these pulses occurs at an optimized "end of access" time. The second pulse occurs at an optimized "end of cycle" time.

Note: For a 200 n/s Storage Unit, the inputs required by section 3.2.6.4.2 will be accomodated by the outputs provided in Section 3.2.6.4.3.

The Crystal Input terminal described in Section 3.2.6.4.1 will accept a standard TCS single-ended input when a logical clocking mechanism is desirable.

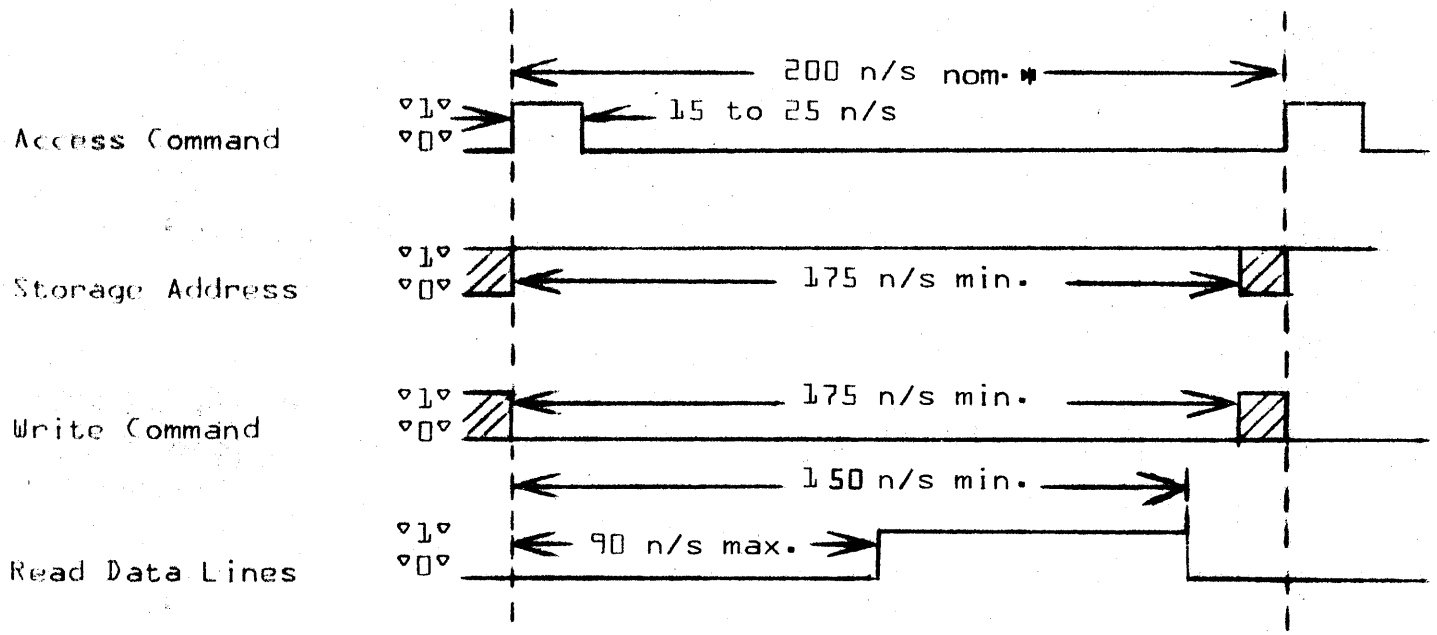


Figure 2a: Read Storage Reference

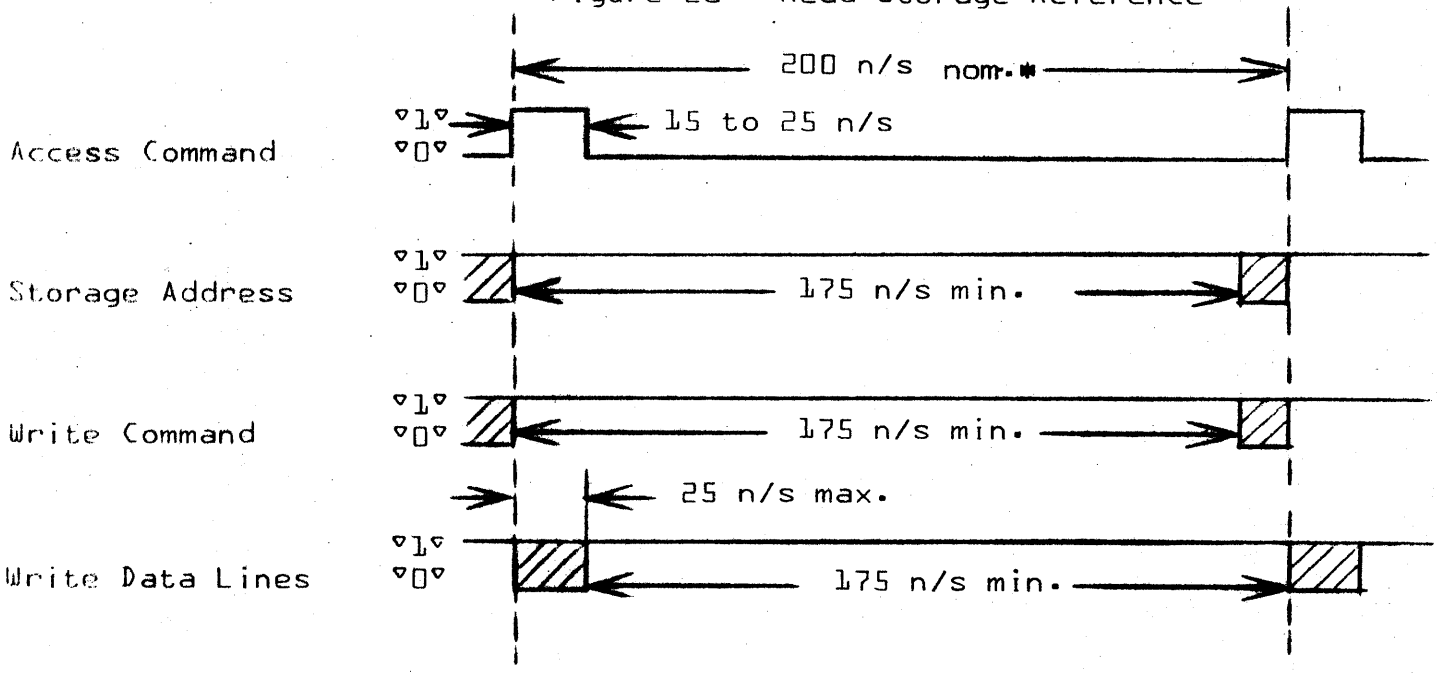


Figure 2b: Write Storage Reference

Figures 2a and 2b: Storage Reference Timing

*Note: Crystal tolerance of .005% will permit the 200 n/s nominal cycle time to decrease to 199.990 n/s, minimum.

3.2.7 Normal Channel Interface

The Normal Channel Interface is defined as the 144 signals which are used to interface the Buffer Controller with a maximum of 16 Normal Input Channels and 16 Normal Output Channels. These signals are implemented using the TCS single-ended transmission scheme described in Engineering Specification 11834700, Section 10.6.1. They are functionally grouped into the three major categories of Output Control, Input Select and Data.

3.2.7.1 Normal Output Channel Control Signals

32 Normal Output Channel control signals are generated by the Control Section and consist of 16 set channel commands and 16 clear channel commands.

3.2.7.1.1 Set Channel Commands

A unique set channel command is generated within the Control Section for each of the 16 possible Normal Output Channels.

A set channel command is nominally an 80 n/s pulse that occurs centered in the 180 n/s channel data pulses. A set channel command occurs only for the specified channel during instructions which require a "ones" or "forced" transfer to a Normal Output Channel. See Figure 3a, page 44, for variations from nominal conditions.

3.2.7.1.2 Clear Channel Command

A unique clear channel command is generated for each of the 16 possible Normal Output Channels.

A clear channel command is nominally an 80 n/s pulse that occurs centered in the 180 n/s channel data pulses. A clear channel command occurs only for the specified channel during instructions which require a "zeroes" or "forced" transfer to a Normal Output Channel. See Figure 3a, page 44, for variations from nominal conditions.

The Normal Output Channels are master cleared by disabling the channel data {forcing zeroes} and simultaneously enabling all sixteen of the clear channel commands. Master Clear on the Normal Channel Interface is performed by the Buffer Controller when a Clear Channel or Master Clear Signal is received on the Station Control Interface, {"ClrChl"; "MC" or "MC-S"} as defined in Section 3.2.9.

3.2.7.2 Channel Select Signals

A unique channel select signal is generated by the Control Section for each of the 16 possible Normal Input Channels. These signals result from continuous translation of the channel designation bit positions (08 through 11) of each word read from storage. Input data must be available from the selected Normal Input Channel within 100 n/s of the leading edge of the channel select signal and remain stable for 60 n/s thereafter. See Figure 3b, page 44.

3.2.7.3 Normal Channel Data

The Normal Channel Data interface provides 4 input terminals per bit, 16 bits parallel, for Normal Input Channel data and 2 output terminals per bit, 16 bits parallel, for Normal Output Channel data.

Use of the input terminals on the part of the Normal Input Channels must be conditioned by the channel select signals previously defined in 3.2.7.2.

Use of the output terminals on the part of the Normal Output Channels must be conditioned by the set channel commands and clear channel commands previously defined in 3.2.7.1.1 and 3.2.7.1.2, respectively.

3.2.7.3.1 Normal Input Channel Data

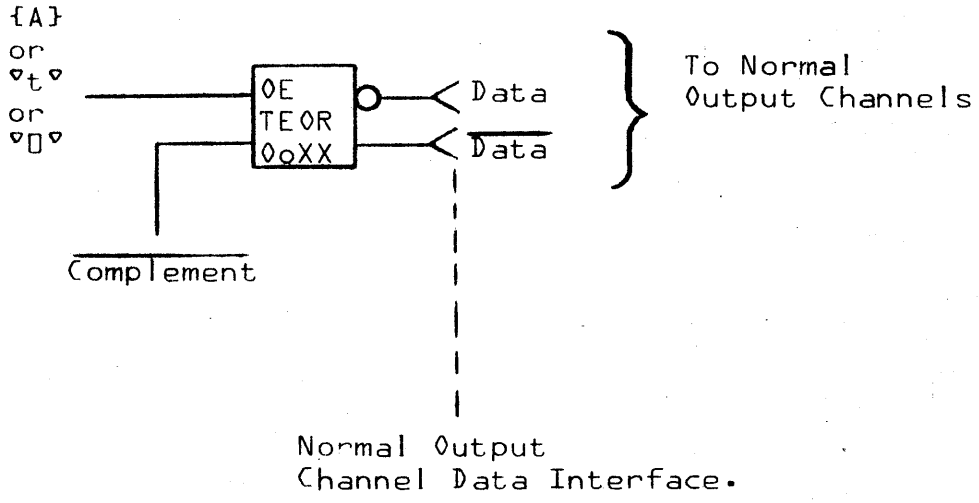
For each of the 16 bit positions, the 4 input terminals on this interface are ▽anded▽ together within the Buffer Controller. As a result of this ▽and▽ fan-in, each input terminal must have the following Boolean expression: ▽(Channel s Data • Channel s Selected) + (Channel s $\overline{\text{Selected}}$)▽. Unused input terminals may be left open (unwired) since an open at the ▽and▽ fan-in will be interpreted as a ▽1▽ level; Channels/Channel bits which are not physically present will be statically translated as $\overline{\text{Selected}}$.

When Normal Input Channel requirements exceed the fan-in capability of this interface, the Normal Input Channels must perform the supplementary fan-in. For an example of how typical Normal Input Channels might utilize this input data interface, see Figure 4 on page 45.

3.2.7.3.2 Normal Output Channel Data

Data to the Normal Output Channels is provided in both the true and negated {1's complement} state for each of the 16 bit positions. Where Normal Output Channel loading requirements exceed the capabilities of these two outputs per bit, the Normal Output Channels must perform the supplementary fan-out.

Each output terminal on this interface may reflect the {A}, the 1's complement of the {A}, the binary decode of a 4-bit designator t, or the 1's complement of the binary decode of a 4-bit designator t. During a Master Clear or Clear Channel operation, each of the 16 output terminals supplying true state data will be forced to a "0" level and each of the 16 output terminals supplying negated {1's complement} state data will be forced to a "1" level.



NOTE: As a result of the Normal Output Channel Data dependency on the translation of each instruction word, the information available on this interface should only be used in conjunction with the Set and Clear Channel Commands.

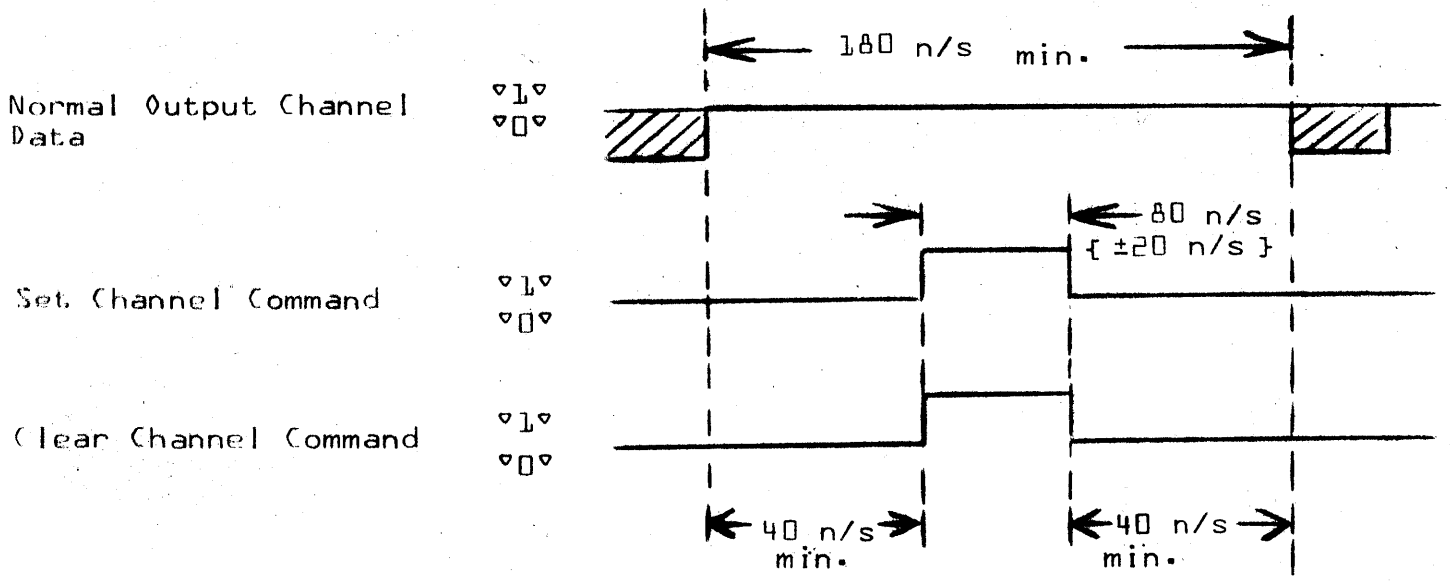


Figure 3a: Normal Output Channel Timing

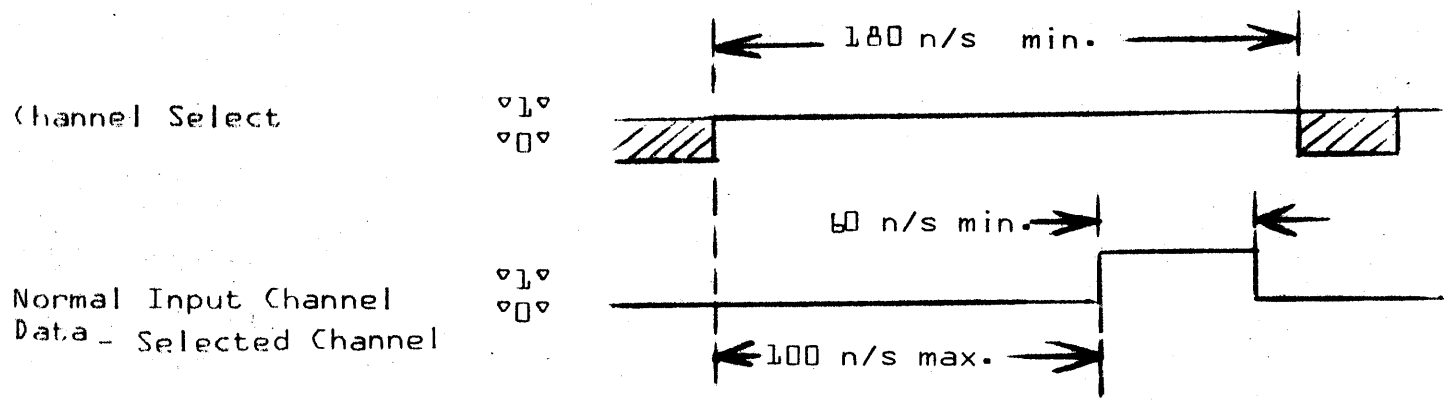


Figure 3b: Normal Input Channel Timing

Figures 3a and 3b: Normal Channel Timing

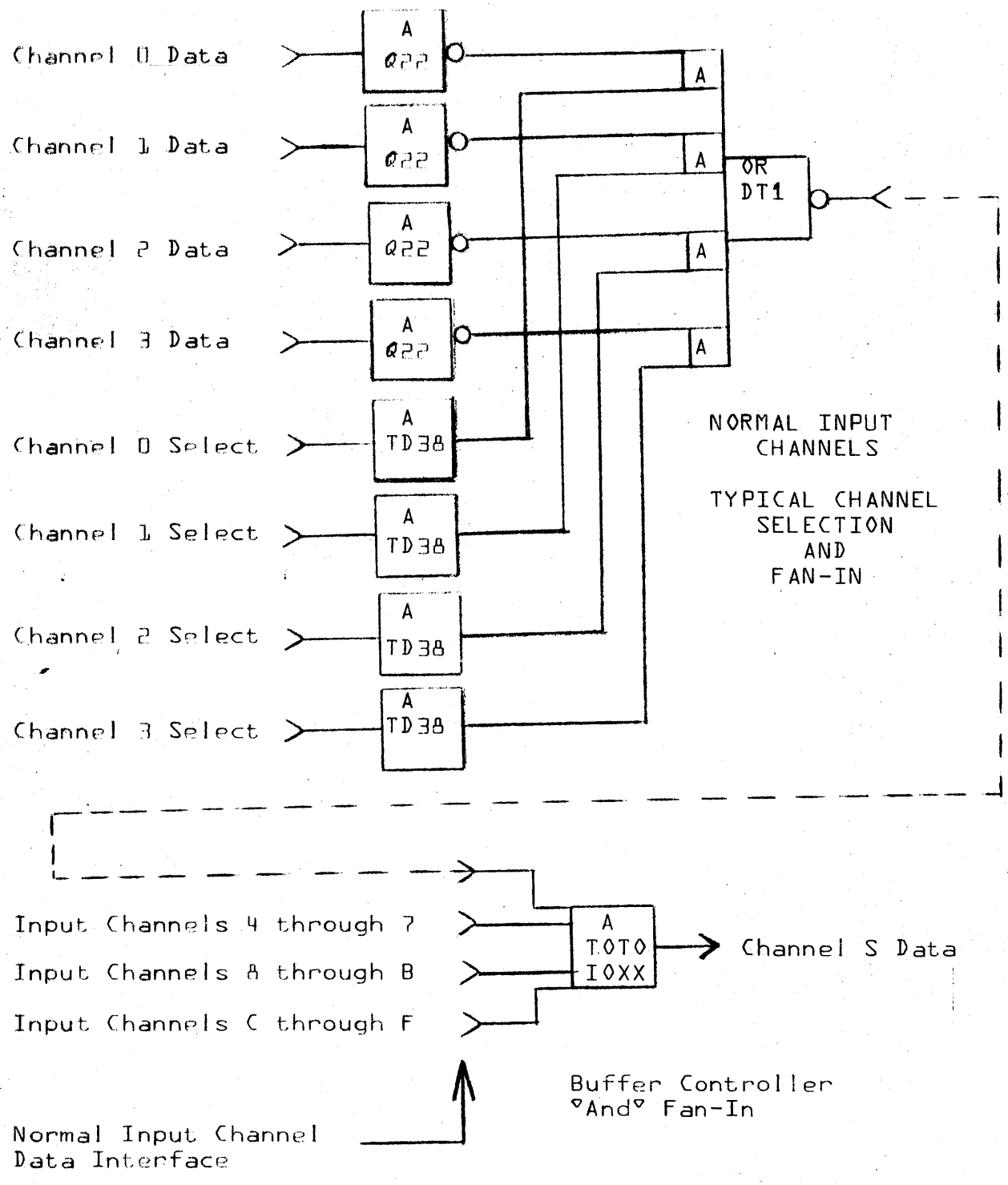


FIGURE 4: TYPICAL NORMAL INPUT CHANNEL CONFIGURATION

1.2.8 Coupler Interface

The Coupler Interface consists of 43 signals which are used to interface the Buffer Controller with a Coupler. These signals are implemented using the TCS single-ended transmission scheme described in Engineering Specification 11834700, Section 10.6.1. They are functionally grouped into the three major categories of Controls to the Coupler, Controls from the Coupler and Data.

When Coupler requirements exceed this single set of interface signals, the Coupler must provide the supplementary fan-in and fan-out facilities. Special purpose control and status signals between the Buffer Controller and the Coupler may be created through the use of Normal Channel facilities. However, it is the responsibility of the Coupler to functionally and physically define these 'auxiliary interface' signals.

1.2.8.1 Controls to the Coupler

1.2.8.1.1 Output Ready

A 15 to 25 n/s pulse from the Control Section of the Buffer Controller, whose leading edge indicates that data from Buffer Controller Storage is ready (deskewed) at the Coupler Interface. This signal occurs during Output Block Transfer instructions only.

1.2.8.1.2 Input Request

A 15 to 25 n/s pulse from the Control Section of the Buffer Controller, whose leading edge indicates that data to Buffer Controller Storage is required at the Coupler Interface. This signal occurs during Input Block Transfer instruction only.

1.2.8.1.3 Parity Strobe

A 15 to 25 n/s pulse from the Control Section of the Buffer Controller whose leading edge serves two purposes. It indicates that the Parity Check signals described in Section 3.2.8.3 are stable. In addition, it indicates that the current input data, being supplied to the interface by the Coupler, has been accepted by the Buffer Controller and is no longer required in a stable state. This signal occurs during Input Block Transfer instructions only.

1.2.8.1.4 Master Clear

This signal provides a means for clearing registers and controls within the Coupler. The Master Clear signal is not originated by the Buffer Controller but is received on the Station Control Interface and repeated by the Control Section for transmission to the Coupler. (See Section 3.2.9 for a description of the Master Clear inputs to the Buffer Controller).

3.2.8.2 Controls from the Coupler

Since Coupler activity is fundamentally asynchronous to the Buffer Controller, the facility for resynchronizing the signals on this interface is included in the Control Section of the Buffer Controller.

3.2.8.2.1 Ready

The Ready Signal is a level indicating in its 'one' state that the Coupler will provide an immediate response for the initial data exchange{s} of an Input Block Transfer or Output Block Transfer instruction. In its 'Zero' state this signal indicates that, on the part of the Coupler, an unpredictable period of time may transpire before the initial data exchange{s} will occur for an Input Block Transfer or Output Block Transfer instruction.

For a description of the effects of this signal on the execution of the Input Block Transfer and Output Block Transfer instructions, see Section 3.2.5.46 and 3.2.5.47, respectively.

Use of this signal is optional to the extent that the Coupler may provide a static 'one' on this line.

3.2.8.2.2 Reply

a 15 to 25 n/s pulse whose leading edge indicates to the Buffer Controller that output data has been accepted by the Coupler or that input data is available from the Coupler. This Control Signal must occur only in response to Output Ready or Input Request Signals from the Buffer Controller. See Section 3.2.8.3.

3.2.8.2.3 Terminate

A 15 to 25 n/s pulse which indicates the termination of an Input Block Transfer or Output Block Transfer instruction on the part of the Coupler. This signal must occur only in place of the Reply.

For a description of the effects of this Signal on Input Block Transfer and Output Block Transfer instructions see Section 3.2.5.46 and 3.2.5.47, respectively.

NOTE: When a Terminate Signal occurs in response to an Input Request Signal, the Buffer Controller will not provide a Parity Strobe Signal.

3.2.8.3 Coupler Data Interface

16 input terminals are available for data transmission from the Coupler to Buffer Controller Storage. Two Parity Check Signals are returned to the Coupler which reflect the odd parity computed by the Buffer Controller for the left-most and right-most bytes received on these 16 input terminals.

16 Output Signals along with 2 Parity bits, one for each byte in the output word, are available for transmission of data from Buffer Controller Storage to the Coupler.

3.2.8.3.1 Coupler Input Data

Data from the Coupler to these 16 input terminals must be stable at the leading edge of the Reply Signal and remain stable until the leading edge of the Parity Strobe Signal.

At the time the input data is written into Buffer Controller Storage, odd parity bits are computed separately in the Buffer Controller for the left-most and right-most byte positions of the 16-bit word. These two parity bits, referred to as Parity Check Signals, are available as outputs to the Coupler for transmission parity checking. The Parity Strobe Signal also provides the timing reference for these Signals.

For timing relationships during input operations from the Coupler, see Figure 5a, page 49.

3.2.8.3.2 Coupler Output Data

Output data to the Coupler, consisting of a 16-bit word and 2 parity bits is provided along with an Output Ready Signal whose leading edge indicates that the data is stable. Output data remains stable until, and for a minimum of 100 n/s after, a Reply or Terminate Signal is received by the Buffer Controller.

At the time each output word is read from Buffer Controller Storage, odd parity bits are computed separately for the right-most and left-most byte positions of the 16-bit word. These Output Parity Signals may be used by the Coupler for transmission parity and are on separate output terminals from the Parity Check Signals described in Section 3.2.8.3.1.

For timing relationships during output operations to the Coupler, see Figure 5b, page 49.

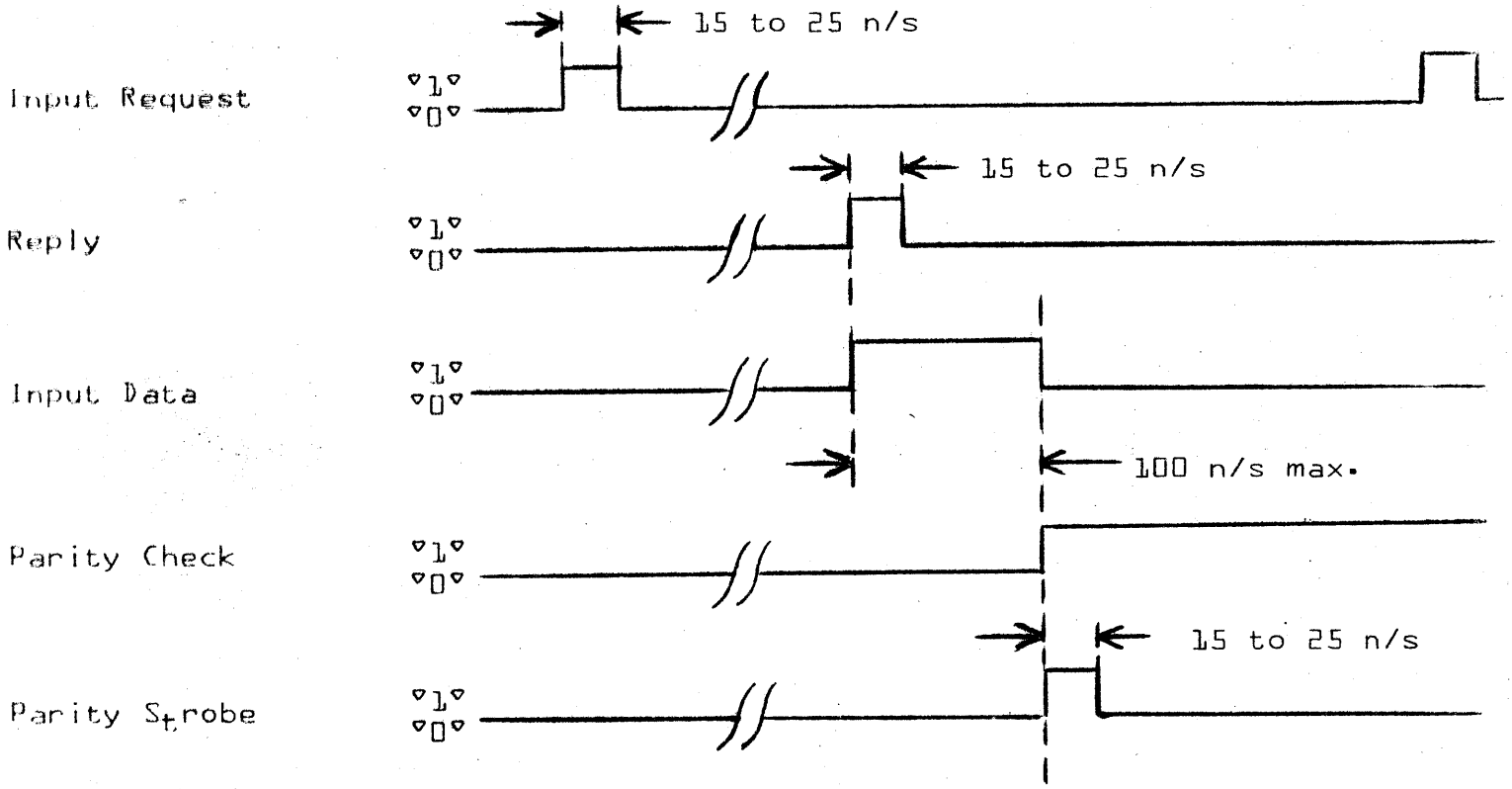


Figure 5a: Input Block Transfer Timing

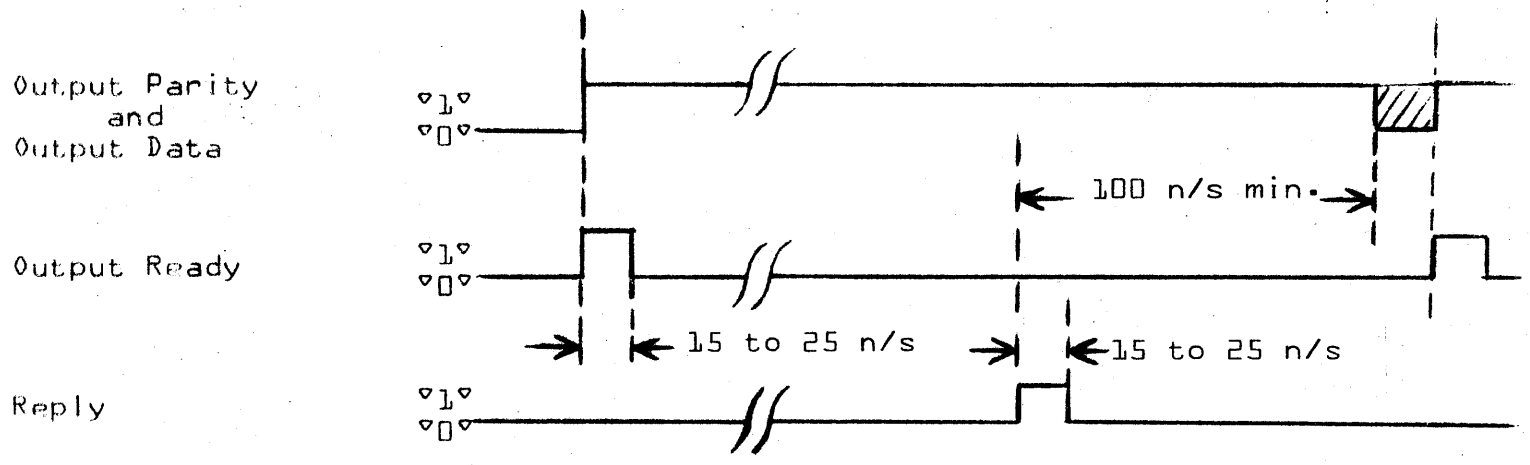


Figure 5b: Output Block Transfer Timing

Figure 5a and 5b: Coupler Interface Timing

{See page 50 for additional comments}

1.2.8.4 Coupler Interface Data Rate

In addition to storage reference cycle time, the data rates on the Coupler Interface are determined by the response time of the Coupler.

In Figure 5a on page 49, the time between the leading edge of the Input Request and leading edge of the Reply is not designated since it is a function of the Coupler. This is also true for Figure 5b on page 45, with respect to the Output Ready and Reply signal timing.

A Reply signal may be received on the Coupler Interface as soon as the leading edge of an Input Request or Output Ready signal occurs; minimum response time may be equal to zero.

The Coupler data rate may be maintained equal to the storage cycle rate, provided the response time of the Reply signal to Input Requests and Output Ready signals is equal to or less than one-half the memory cycle time minus 60 n/s.

For a 200 n/s Storage Unit the maximum allowable response time for each Reply would be 40 n/s in order to maintain a 5 MHZ data rate.

For a 1.1 u/s Storage Unit the maximum allowable response time for each Reply would be 490 n/s in order to maintain a 909 KHZ data rate.

Maintaining the Coupler data rate equal to the storage cycle rate is contingent on keeping each Reply response time within the timing constraints of the crystal such that resynchronization of the Reply is not required.

When the response time of any Reply signal exceeds the timing constraints of the crystal, storage reference cycles for the remainder of that Block Transfer instruction are performed in an "on demand" mode, asynchronous to the crystal. Resynchronization with the crystal is performed only at the completion of such a Block Transfer Instruction and may require one additional storage reference cycle time, maximum.

The "on demand" mode of operation initiates storage reference cycles whenever a Reply signal is received on the Coupler Interface and an End of Cycle {Storage Not Busy} signal is received on the Storage Interface for any previously initiated storage reference cycle. Since this mode of operation does not use the crystal for its time base but depends on the End of Cycle signal {a delayed Access Command}, then an additional 35 n/s per storage reference cycle must be allowed for worst case component tolerances.

Resynchronization of Terminate signals is unconditional and requires from one storage reference cycle time minimum to 1.5 storage reference cycle times maximum.

3.2.9 Station Control Interface

The Station Control Interface consists of 123 signals and provides the facilities for externally controlling and monitoring certain Buffer Controller operations. These signals are implemented using the TCS single-ended transmission scheme described in Engineering Specification 11834700. Throughout this specification the "negative logic" convention described in Section 6.4 of Engineering Specification 11834700 is directly applicable. However: "Open" inputs will be interpreted as logical "1's" for only those signals where it is so described; "Grounded" inputs are permissable for interpretation as logical "0's" for only those signals where it is so described.

3.2.9.1 Pluggable Station Control Signals

116 signals are available at the contacts of four 61-pin connectors in order to provide pluggability for these key signals.

The pluggable nature of this substantial portion of the Station Control Interface enhances manufacturability and maintainability of the Buffer Controller as a component. Standardization of these features is assured only to the extent that Station utilization of this interface maintains its integrity. Since these signals already represent an optimized, minimal concession for Buffer Controller maintenance, their availability (direct or indirect) for this purpose is vital.

The inputs to the Buffer Controller from this pluggable control interface will be interpreted as ones when left open and will be interpreted as zeroes when grounded except where otherwise stated.

NOTE: The TCS single-ended transmission scheme requires a 100 ohm characteristic impedance which is maintained in the wiring by twisting each signal wire with a ground wire: 116 signals + 116 grounds = 232 connector contacts. Three contacts in each 61-pin connector are unused: 58 x 4 = 232 connector contacts.

3.2.9.1.1 ▽A▽ Register Entry {SETA00 through SETA15, CLR-AR}

Each of the 16 bit positions in A may be separately set by the appropriate input signal on this interface. The 17th input signal clears all of the bits in A.

These input signals are effective at the zero level or when the input terminal is grounded through a series resistance of 100 ohms, {These input terminals must not be grounded directly}. When set and clear inputs occur simultaneously, the {A} are undefined.

3.2.9.1.2 ▽P▽ Register Entry {SETP00 through SETP15, CLEARP}

Each of the 16 bit positions in P may be separately set by the appropriate input signal on this interface. The 17th input signal clears all of the bits in P.

These input signals are effective at the zero level or when the input terminal is grounded through a series resistance of 100 ohms, {These input terminals must not be grounded directly}. When set and clear inputs occur simultaneously the {P} are undefined.

The Storage Address Register, S, also receives these signals and reacts identically to the P Register with respect to this interface.

3.2.9.1.3 Adder Display {REG-00 through REG-15}.

These 16 status output signals reflect the sum being formed by the Adder in the Buffer Controller Arithmetic Section.

See Sections 3.2.9.1.5 through 3.2.9.1.13 for a description of Augend and Addend inputs to the Adder.

3.2.9.1.4 ▽P▽ Register Display {PRS-00 through PRS-15}

These 16 status output Signals reflect the {P}. If, during the course of program execution, the Buffer Controller is stopped, the {P} will always be one greater than the address of the current instruction.

3.2.9.1.5 A Register Select {SEL-AR}

When the Buffer Controller is stopped, a logical one on this input terminal will cause the {A} to be statically enabled to the Adder as an Augend input.

3.2.9.1.6 S Register Select {SEL-SR}

When the Buffer Controller is stopped, a logical one on this input terminal will cause the {S} to be statically enabled to the Adder as an Augend input.

3.2.9.1.7 B1 Register Select {SEL-B1}

When the Buffer Controller is stopped, a logical one on this input terminal will cause the {B1} to be statically enabled to the Adder as an Augend input.

3.2.9.1.8 B2 Register Select {SEL-B2}

When the Buffer Controller is stopped, a logical one on this input terminal will cause the {B2} to be statically enabled to the Adder as an Augend input.

3.2.9.1.9 Not X Register Select {SEL-NX}

When the Buffer Controller is stopped a logical one on this input terminal will cause the 1's complement of the {X} to be statically enabled to the Adder as an Addend input. NOTE: The Exchange Register, X, contains the one's complement of the data read from Storage.

3.2.9.1.10 X Register Select {SEL-XR}

When the Buffer Controller is stopped a logical one on this input terminal will cause the {X} to be statically enabled to the Adder as an Addend input.

3.2.9.1.11 "t" Designator Select {SEL-T}

When the Buffer Controller is stopped a logical one on this input terminal will cause the 16-bit translation of the "t" designator to be statically enabled to the Adder as an Addend input. NOTE: This 16-bit translation consists of 15 zeroes and a one with the one appearing in the bit position designated by the "t" field of the last word read from Storage.

3.2.9.1.12 Not "t" Designator Select {SEL-NT}

When the Buffer Controller is stopped a logical one on this input terminal will cause the 1's complement of the 16-bit translation of the "t" designator to be statically enabled to the Adder as an Addend input.

3.2.9.1.13 Augend and Addend Not Selected {ADDOFF}

When the Buffer Controller is stopped, a logical one on this interface will enable addend and augend inputs to the adder to be determined by the instruction function and cycle translations. Whenever adder inputs are selected by means of the signals described in 3.2.9.1.5 through 3.2.9.1.12 then this signal must be a logical zero in order to prevent the Buffer Controller from internally enabling addend and/or augend inputs.

Note: When the Buffer Controller is running, the input signals described in Sections 3.2.9.1.5 through 3.2.9.1.13 have no effect.

3.2.9.1.14 Breakpoint Address {BKP-00 through BKP-15}

These 16 input lines are compared to the instruction and operand addresses within the Buffer Controller. In the event of a comparison, the Buffer Controller will inspect the input signals described in sections 3.2.9.1.15 and 3.2.9.1.16 to determine if a breakpoint stop should occur.

3.2.9.1.15 Breakpoint Instruction Select {$\overline{\text{BPI}}$}

When this input signal is a logical zero, and a comparison exists between the current instruction address and the Breakpoint Address inputs, then the Buffer Controller will stop at the end of the current storage reference cycle.

3.2.9.1.16 Breakpoint Operand Select {$\overline{\text{BPO}}$}

When this signal is a logical zero, and a comparison exists between the current operand address and the Breakpoint Address inputs, then the Buffer Controller will stop at the end of the current storage reference cycle.

Note: Following a breakpoint stop, Buffer Controller operation may be resumed through the use of GO input{s} on the Station Control Interface. See Sections 3.2.9.1.20 and 3.2.9.2.1.

3.2.9.1.17 Parity Error {PE-ID}

This output status line provides, at the logical one level, a Buffer Controller storage parity error indication. For each storage reference cycle that reads a 16-bit word, the parity bit for that word is checked for correctness within the Buffer Controller. This parity check occurs unconditionally and once an error has been detected, it is stored in the parity error flip-flop. Once set, the parity error flip-flop, which drives this output status line, will remain at the one level until a Master Clear or Parity Error Clear is performed.

3.2.9.1.18 Parity Error Clear {$\overline{\text{CLR-PE}}$}

A logical zero on this input terminal will result in the application of a clear {reset} signal to the parity error flip-flop which provides the status described in Section 3.2.9.1.17.

Note: If this input terminal is left at the zero level continuously, parity error status {Section 3.2.9.1.17} will consist of a 10 to 30 n/s pulse for each memory reference cycle in which a parity error occurs.

3.2.9.1.19 Stop On Parity Error Select {$\overline{\text{EN-PE}}$}

A logical zero on this input terminal will cause the Buffer Controller to stop at the end of any storage reference cycle in which a parity error is detected. This stop, when selected, is contingent on parity error detection, not on parity error status. Thus, the Buffer Controller will not stop for parity errors which occurred prior to the time this input terminal went to the zero level.

3.2.9.1.20 Go Switch Inputs {GO-S and $\overline{\text{GO-S}}$}

Two input terminals are provided for interfacing the break-before-make contacts of a "GO" switch with the control section of the Buffer Controller. One terminal is intended for connection to the normally closed contact of the switch, is normally at the zero level and is referred to as the "GO" input. The other terminal is intended for connection to the normally open contact of the switch, is normally at the one level, and is referred to as the "$\overline{\text{GO}}$" input. For each depression of this make-before-break switch, the control section of the Buffer Controller will resynchronize the switch action and begin performing storage reference cycles. The state of the switch is monitored so that irrespective of contact bounce, the switch contacts must be returned to their normal state before the GO operation may be repeated. Depression of the switch while the Buffer Controller is already running will have no effect.

3.2.9.1.21 Stop Switch {$\overline{\text{STOP-S}}$}

At the logical zero level this input will cause the Buffer Controller to stop at the end of the current instruction. This input signal is resynchronized by the control section of the Buffer Controller and will result in an "Instruction Step" mode of operation if left at the zero level during GO operations.

3.2.9.1.22 Master Clear Switch {$\overline{\text{MC-S}}$}

At the logical zero level this input will result in stopping the Buffer Controller and causing a clear of its controls and addressable {A, B1, B2, and P} registers. This input is repeated for transmission on the Storage, Normal Channel, and Coupler Interfaces, as described in Sections 3.2.6.1.3, 3.2.7.1.2, and 3.2.8.1.4, respectively.

This signal is not resynchronized and may cause storage parity errors unless utilized only when the Buffer Controller is stopped. This statement is also true for the 34 signals defined in Sections 3.2.9.1.1 and 3.2.9.1.2, the A and P Register Entry inputs.

3.2.9.1.23 Instruction Step {$\overline{\text{INSTRS}}$}

This input signal is identical to the Stop Switch input described in Section 3.2.9.1.21.

3.2.9.1.24 Cycle Stop {$\overline{\text{CYCLES}}$}

This input signal is identical to the Stop Switch input described in Section 3.2.9.1.21 with the exception that the resynchronization is performed such that the Buffer Controller will stop at the end of the current storage reference cycle regardless of its relationship to the end of the current instruction.

3.2.9.1.25 Enter Mode {$\overline{\text{ENTER}}$}

When this input signal is a logical zero, each storage reference cycle performed by the Buffer Controller transfers the {P} to the Storage Address Register, S; stores the {A} at the location designated by {S}; and increases the {P} by one. The function translations are disabled {forced to zeroes} so that in all other respects the Buffer Controller executes a Selective Stop instruction as described in Section 3.2.5.1.

Note: This input is not resynchronized and should not change state while the Buffer Controller is running.

3.2.9.1.26 Sweep Mode {$\overline{\text{SWEEP}}$}

When this input signal is a logical zero, each storage reference cycle performed by the Buffer Controller transfers the {S} plus one to the P and S registers; reads the contents of the storage location designated by the {S}; and transfers the 1's complement of the storage word to the Exchange Register, X. {For the first storage reference cycle after the P and S Registers have been cleared, the increment of these registers is disabled in order to maintain correspondence between these address registers and the {X}}. The function translations are disabled {forced to zeroes} so that in all other respects the Buffer Controller executes a Selective Stop instruction as described in Section 3.2.5.1.

Note: This input is not resynchronized and should not change state while the Buffer Controller is running.

3.2.9.1.27 Selective Stop {NOP—00}

When this input is a logical zero the Selective Stop instruction described in Section 3.2.5.1 will result in a stop at the end of the current storage reference cycle. A logical one on this input terminal will cause the selective stop instruction to be interpreted as a no-op according to the description in Section 3.2.5.1.

Note: This signal is not resynchronized and should not change state while the Buffer Controller is running.

3.2.9.1.28 Clear Channel {$\overline{\text{CLRCHL}}$}

A logical zero on this input terminal will result in a clear of the Normal Output Channels as described in Section 3.2.7.1.2.

3.2.9.1.29 Timing Margins {$\overline{\text{SLOW—A}}$, $\overline{\text{FAST—A}}$, $\overline{\text{SLOW—B}}$, $\overline{\text{FAST—B}}$}

Four input terminals are provided which, at the logical zero level, impose timing margins on operations internal to the Buffer Controller as well as timing variances on its interfaces.

The use of timing margins tends to simulate "worst case" conditions within the Buffer Controller. If the distribution of the circuits in key areas of the Buffer Controller are such that a "worst case" condition exists with normal timing, then the Buffer Controller cannot be assumed to run reliably under timing margins. The use of timing margins is intended to identify the areas where "worst case" conditions exist so these potential problem areas can be investigated as maintenance time permits.

When the $\overline{\text{SLOW—A}}$ input terminal is at a zero level, internal timing pulses which occur over the first half of each storage reference cycle are increased in width and distributed over a longer period by approximately 8%.

When the $\overline{\text{FAST—A}}$ input terminal is at a zero level, internal timing pulses which occur over the first half of each storage reference cycle are decreased in width and distributed over a shorter period by approximately 8%.

When the $\overline{\text{SLOW-B}}$ input terminal is at a zero level, internal timing pulses which occur over the second half of each storage reference cycle are increased in width and distributed over a longer period by approximately 8%.

When the $\overline{\text{FAST-B}}$ input terminal is at a zero level, internal timing pulses which occur over the second half of each storage reference cycle are decreased in width and distributed over a shorter period by approximately 8%.

The use of timing margins does not affect the frequency of storage reference cycles except in the case of Block Transfer Instructions for which the crystal-controlled frequency cannot be maintained by the Coupler.

3.2.9.1.30 Not Running Status {$\overline{\text{RUN-ID}}$}

At the one level this output status signal indicates that the Buffer Controller is stopped. In this state, Buffer Controller operation may be initiated only through the use of one of the GO operations defined in Sections 3.2.9.1.20 and 3.2.9.2.1.

3.2.9.1.31 RNI Status {RNI-ID}

At the one level this output status signal indicates that the current storage reference cycle is for the purpose of reading an instruction.

3.2.9.1.32 RADR Status {RAD-ID}

At the one level this output status signal indicates that the current storage reference cycle is for the purpose of reading an address during the execution of an instruction which specifies indirect addressing.

3.2.9.1.33 ROP Status {ROP-ID}

At the one level, this output status signal indicates that the current storage reference cycle is for the purpose of reading an operand.

3.2.9.1.34 STO Status {STO-ID}

At the one level this output status signal indicates that the current storage reference cycle is for the purpose of storing an operand.

Note: The RNI, RADR, and ROP status signals defined in Sections 3.2.9.1.32 → 3.2.9.1.33, respectively, are unconditionally at the zero level when the Buffer Controller is stopped and the "Augend and Addend Not Selected" input defined in Section 3.2.9.1.13 is at the zero level.

3.2.9.1.35 Jump Condition Met Status {JPM-ID}

At the one level this output status signal indicates the current instruction is a Jump and that the conditions for the Jump to occur are satisfied. During an Unconditional Jump, this signal is unconditionally at the one level.

3.2.9.2 Non-Pluggable Station Control Signals

These 7 signals are physically available on the Buffer Controller backpanel, use the single-ended transmission scheme described in Engineering Specification 11834700, and interpret open inputs as logical ones. Grounded inputs will be interpreted as logical zeroes unless otherwise specified.

3.2.9.2.1 Not Go {$\overline{GO}$}

At the logical zero level this signal constitutes a GO command to the Buffer Controller. The signal is resynchronized and results in the initiation of Buffer Controller storage reference cycles. This input is monitored by the Buffer Controller such that it must be returned to the one level before the GO operation may be repeated. No allowance is made for contact bounce since it is not intended for direct connection to a switch.

Note: This signal interacts with the facility described in Section 3.2.9.1.20 to the extent that its usage is constrained to the time when the GO switch contacts are in their normal {switch released} positions or, where the switch is not used, the inputs are biased to simulate the normal positions.

3.2.9.2.2 Not Stop {$\overline{STOP}$}

This input signal is functionally identical to the Stop Switch Input described in Section 3.2.9.1.21.

3.2.9.2.3 Not Master Clear {$\overline{MC}$}

This input signal is functionally identical to the Master Clear Switch Input described in Section 3.2.9.1.22.

3.2.9.2.4 Enable Storage Write {$\overline{DIS-ST}$}

At the zero level this input signal prevents the transmission of the Write Command on the Storage Interface as defined in Section 3.2.6.1.2.

This signal is not resynchronized and may result in Storage Parity Errors unless its state is changed only when the Buffer Controller is stopped or when the Buffer Controller is performing a storage reference cycle for which the Write Command is unused.

3.2.9.2.5 Not Force Function {$\overline{\text{FORCEF}}$}

Prior to the utilization of this input signal at the zero level, the Buffer Controller must be Stopped and Master Cleared, in that order.

At the zero level this signal results in forcing the Function translations to an FX00, Input Block Transfer or Output Block Transfer instruction. In addition, bit positions 00 through 03 of A are forced to the one state so that a word count of 4,096 is designated as a maximum block length.

At the time a GO operation is performed, {see Sections 3.2.9.1.20 and 3.2.9.2.1}, the Buffer Controller will perform an RNI storage reference cycle without changing the Function translations so that an Input Block Transfer or Output Block Transfer instruction will be executed exactly as described in Sections 3.2.5.46 and 3.2.5.47 respectively.

During the time this input signal is at the zero level, the Force Function Select input described in Section 3.2.9.2.6 determines whether an Input Block Transfer or Output Block Transfer will be forced.

Note: Prior to the GO command, the Ready input on the Coupler interface should be at a one level to prevent an immediate exit from the Block Transfer instruction. Prior to the completion of the Block Transfer, this $\overline{\text{FORCEF}}$ input terminal should be returned to the one level to prevent an immediate repetition of the Block Transfer instruction simulation. The End of Block Transfer Status signal described in Section 3.2.9.2.7 occurs 100 n/s prior to the latest time possible for returning the $\overline{\text{FORCEF}}$ input terminal to the "one" level without repeating the I/O operation. The $\overline{\text{FORCEF}}$ input signal may consist of a 10 n/s minimum, zero-going pulse. This input terminal must not be directly grounded.

3.2.9.2.6 Force Function Select {EN-OUT}

During the time the Not Force Function input, described in Section 3.2.9.2.5, is at the zero level, the Force Function Select input determines whether an Input Block Transfer or Output Block Transfer Instruction will be forced. When this input terminal is grounded {or at a zero level} the Not Force Function zero-going input will result in an Input Block Transfer. When this input terminal is open {or at a one level}, the Not Force Function zero-going input will result in an Output Block Transfer.

3.2.9.2.7 End of Block Transfer Status {EOP-CC}

This output status line consists of a 15 to 25 n/s pulse which occurs at the end of each Input and Output Block Transfer instruction.

This pulse accompanies the last Output Ready signal on the Coupler Interface {Section 3.2.8.2.1} for each Output Block Transfer Instruction {Section 3.2.5.47}. Whenever output data is rejected on the Coupler Interface through the use of a Terminate signal {Section 3.2.8.2.3}, this pulse will also occur during the resultant exit from the Output Block Transfer instruction.

During Input Block Transfer instructions this pulse occurs after a Terminate signal, or a Reply signal for the final Input Request, has been received on the Coupler Interface. The End of Block Transfer Status pulse occurs at the time an additional Input Request would have occurred had the Input Block Transfer Instruction not performed an exit.

3.3 Physical Requirements

The Buffer Controller consists of one backpanel and 17 50-PAKs of Register and Control logic. The backpanel includes wiring designated by logic, power, connector, plug, and hand-tab wire lists.

Chassis space, D.C. power, and forced air cooling must be provided by the equipment/cabinetry in which the Buffer Controller serves as a component.

The Buffer Controller requires a 4096, 18-bit word Storage Unit as a minimal addition, in order to achieve its intended functions as a programmable, master control element.

3.3.1 Backpanel and 50-PAKs

The 26 50-PAK position backpanel will accommodate, in addition to the 17 50-PAKs of Buffer Controller logic, 8 Normal Input Channels on 2 50-PAKs, 8 Normal Output Channels on 4 50-PAKs, and Coupler/Station logic on 3 50-PAKs.

The backpanel is approximately 14 inches high by 14 inches wide. An allowance of 10'' in depth will accommodate the backpanel with inserted 50-PAKs and backpanel wiring.

The Backpanel with 50-PAKs, wiring and connectors/plugs weighs approximately 35 lbs., uncrated.

3.3.1.1 Materials/Workmanship

The following documents shall apply:

Engr/CDC Spec.	Title
20277200	Three-layer Printed Circuit Board
11828700	General Quality Specification for Intebrid and Integrated Circuits
11845900	Workmanship Specification for CDC Manufactured Intebrid Circuits
10120300	General Quality Requirements
52302000	Performance Specification for Connector Plates

3.3.2.2 Interchangeability

Of the 17 50-PAKs of Register and Control logic there are 9 unique types. Since four of these unique types are used more than once, their interchangeability within the Buffer Controller should be exploited for maintenance/manufacturing checkout purposes.

The FR101 proper is not directly interchangeable with any previous programmed controller including the FF406.

3.3.2 Interfaces

In order to standardize the Storage, Normal Channel, Coupler and Station Control Interfaces into a physical as well as logical configuration, the mechanical connections to these interfaces have been extended beyond the 17 50-PAK locations occupied by the Buffer Controller proper, for a majority of these signals.

3.3.2.1 Storage Interface

The Storage Interface signals are available on two 61-pin plugs with the signal allocation shown in Tables 4 and 5 on pages 67 and 68, respectively.

The left-most 4 bits of the 16-bit Storage Address are not available on the 61-pin plugs which accommodate all other Storage Interface signals. These Address bits are available on the backpanel as described in Table 14 on page 80.

3.3.2.2 Coupler Interface

Coupler Interface signals are available at backpanel 50-PAK locations outside of the 17 50-PAK locations occupied by the Buffer Controller proper. The allocation of these signals is shown in Table 6 on Pages 69 and 70.

3.3.2.3 Normal Channel Interface

Normal Channel Controls and Data for Input and Output Channels 0 through 7 are available at backpanel 50-PAK locations outside of the 17 50-PAK locations occupied by the Buffer Controller proper. The allocation of these signals is shown in Table 7 on Pages 71, 72 and 73.

Normal Channel Controls and Data for Input and Output Channels 8 through F are available at backpanel 50-PAK locations occupied by the Buffer Controller, proper. The allocation of these signals is shown in Table 8 on Pages 74 and 75.

3.3.2.4 Station Control Interface

Pluggable Station Control Interface signals are available on four 61-pin connectors with the signal allocation shown in Tables 9 through 12 on Pages 76 through 79.

Non-pluggable Station Control Interface signals are available at backpanel 50-PAK locations occupied by the Buffer Controller proper. The allocation of these signals is shown in Table 13 on Page 80.

3.4 Power

The following voltages at the indicated amperages are required by the 17 50-PAKs of Buffer Controller logic.

Nominal Requirements	Worst Case Component Tolerances and ±10% Voltage Margins
-6.0V @ 76A	-6.6V @ 102A
-2.0V @ 26.7A	-2.2V @ 32A
+6.0V @ 3A	+6.6V @ 4A
1,725 BTU/Hr.	2,500 BTU/Hr.

These requirements include an allowance of -6V @ 2A, -2V @ 1A, and +6V @ 4A for a pluggable maintenance console. See Engineering Specification 58018900.

These voltages are available on the female contacts of Power Connector J1 with +6V on contact #1, -6V on contact #2, -2V on contact #3 and ground on contacts #4 and #5.

3.5 Environmental Requirements

The requirements of Engineering Standard 1.30.011, section 3.12 shall be met.

For the operating state temperature range of 40-120°F the following minimum air velocity and volume is required.

1000 linear feet per minute

250 cubic feet per minute

3.6 MTBF

The MTBF goal for the Buffer Controller {excluding Storage, Normal Channels, and Coupler} shall be 36,000 hours.

3.7 MTTR

With the maintenance philosophy based on repair through replacement of the smallest pluggable component, the MTTR for the Buffer Controller is estimated at .6 hours.

3.8 Useful Life

Buffer Controller failure mechanisms are primarily of a random catastrophic nature, {solder connections, Intebrids, etc.,}. 50-PAK connectors/backpanel contacts have a useful life of 500 cycles, {50-PAK removal and insertion}, minimum per 50-PAK location.

Implementation of the Buffer Controller as a component will result in additional useful life factors {motors, switches, etc.} which are outside the scope of this specification.

4.0 TEST REQUIREMENTS

Modular test should include the exchange of 50-PAKs by type, such that the entire Normal Channel Interface may be tested using only those facilities for Channels 0 through 7.

Modular test should employ an ▽Echo▽ Coupler as a test fixture for the purpose of checking-out the Coupler Interface.

5.0 PREPARATION FOR DELIVERY

The requirements of CDC-SPEC 10120300 shall apply as described in the Packaging Section. The Buffer Controller shall be considered as a Class A-1 item with respect to packaging requirements.

Storage Interface Plug 1 (P01)

Connector Pin	Signal Name	Function
A1/A2	SRM-04	Storage Address, Bit 04
A3/A4	05	05
A5/A6	06	06
A7/A8	07	07
A9/A10	08	08
B1/B2	SRM-09	Storage Address, Bit 09
B3/B4	10	10
B5/B6	11	11
B7/B8	12	12
B9/B10	13	13
C1/C2	SRM-14	Storage Address, Bit 14
C3/C4	SRM-15	Storage Address, Bit 15
C5/C6	ST0-00	Write Data, Bit 00
C7/C8	01	01
C9/C10	02	02
D1/D2	ST0-03	Write Data, Bit 03
D3/D4	04	04
D5/D6	05	05
D7/D8	06	06
D9/D10	07	07
E1/E2	ST0-08	Write Data, Bit 08
E3/E4	09	09
E5/E6	10	10
E7/E8	11	11
E9/E10	12	12
F1/F2	ST0-13	Write Data, Bit 13
F3/F4	14	14
F5/F6	15	15
F7/F8	16	16

NOTE: All signals are differential with true state levels on odd numbered pins and negated levels on even numbered companion pins.

Table 4: Storage Interface P01

Storage Interface Plug 2 (P02)

Connector Pin	Signal Name	Function
A1/A2	SPARE	
A3/A4	SPARE	
A5/A6	ST0-50	Read Data , Bit 00
A7/A8	↓ 51	↓ 01
A9/A10	↓ 52	↓ 02
B1/B2	ST0-53	Read Data , Bit 03
B3/B4	↓ 54	↓ 04
B5/B6	↓ 55	↓ 05
B7/B8	↓ 56	↓ 06
B9/B10	↓ 57	↓ 07
C1/C2	ST0-58	Read Data , Bit 08
C3/C4	↓ 59	↓ 09
C5/C6	↓ 60	↓ 10
C7/C8	↓ 61	↓ 11
C9/C10	↓ 62	↓ 12
D1/D2	ST0-63	Read Data, Bit 13
D3/D4	↓ 64	↓ 14
D5/D6	↓ 65	↓ 15
D7/D8	↓ 66	↓ 16 (P.B.)
D9/D10	SPARE	
E1/E2	XTAL	Crystal Input
E3/E4	TOXTAL	Crystal Feedback
E5/E6	ST0-RQ	Access Command
E7/E8	V055	End of Access to Storage
E9/E10	WRITE	Write Command
F1/F2	V010	End of Cycle to Storage
F3/F4	MC-ST0	Master Clear to Storage
F5/F6	E0A	End of Access from Storage
F7/F8	E0C	Enc of Cycle from Storage

NOTE: Differential signals have their true state on odd numbered pins and negated levels on even numbered companion pins. Single-ended signals are on odd numbered pins with ground on even numbered companion pins.

Table 5: Storage Interface P02

Coupler Interface: Data and Controls to the Coupler

50-PAK Location	Connector Pins	Signal Name	Function
A1A00	D3/22	CC0-00	Coupler Output Data, Bit 00
	F3/33	01	01
	F2/32	02	02
	B1/14	03	03
	G3/A2	04	04
	G2/A5	05	05
	I3/E5	06	06
	M2/M5	07	07
A1B00	D3/13	CC0-08	Coupler Output Data, Bit 08
	F3/A2	09	09
	F2/A5	10	10
	B1/01	11	11
	G3/65	12	12
	G2/B5	13	13
	I3/G5	14	14
	M2/N5	15	15
A1A00	L3/K5	CC0-16	Coupler Output Parity, Bit 16
A1B00	L3/L5	CC0-17	Coupler Output Parity, Bit 17
A1A01	T0/E4	OUTRDY	Output Ready to the Coupler
A1A01	H0/C4	INPREQ	Input Request to the Coupler
A1A00	N3/05	CK-PAR	Parity Strobe to the Coupler
A1A01	L2/J5	MC-CC	Master Clear to the Coupler

NOTE: All signals are TCS single-ended with connector pins to the left of the slash/asterisk designated as the signal pins and the companion contacts to the right of the slash/asterisk designated as ground.

Table 6: Coupler Interface, Output

Coupler Interface: Data and Controls from the Coupler (Parity bits to the Coupler based on Input Data)

GO-PAK Location	Connector Pins	Signal Name	Function
A1A00	G0⋈A1 F0⋈30 G1⋈A4 K1⋈H4 M0⋈L4 M1⋈M4 W1⋈54 V0⋈50	CCI-00 01 02 03 04 05 06 07	Coupler Input Data, Bit 00 01 02 03 04 05 06 07
A1B00	G0⋈C4 F0⋈A1 G1⋈B4 K1⋈J4 M0⋈04 M1⋈N4 W1⋈51 V0⋈41	CCI-08 09 10 11 12 13 14 15	Coupler Input Data, Bit 08 09 10 11 12 13 14 15
A1A01 A1A01	D2/25 I2/D5	CCI-16 CCI-17	Computed Parity: Left-most Input byte Computer Parity: Right-most Input byte
A1A01 A1A01 A1A01	B2⋈15 E2⋈35 C2⋈12	CREADY CREPLY CCTERM	Ready from the Coupler Reply from the Coupler Terminate from the Coupler

NOTE: All signals are TCS single-ended with connector pins to the left of the slash/asterisk designated as the signal pins and the companion contacts to the right of the slash/asterisk designated as ground.

Table 6A: Coupler Interface, Input

Normal Input Channels 0 → 7: Select and Data Interface

50-PAK Location	Connector Pins	Signal Name	Function
A1A12	B1⋈14	SEL-I0	Select Normal Input Channel 0
	G0⋈A1	I1	1
	M1⋈M4	I2	2
	R0⋈V4	I3	3
A1B12	B1⋈01	I4	4
	G0⋈C4	I5	5
	M1⋈N4	I6	6
	R0⋈X4	I7	7
A1A12	C1⋈11	I03-00	Normal Input Channels 0-3, Data Bit 00
	C0⋈10	01	01
	T1⋈Z4	02	02
	N0⋈04	03	03
	H0⋈C4	04	04
	I1⋈D4	05	05
	S0⋈X4	06	06
	N1⋈N4	07	07
	H3⋈C5	08	08
	G2⋈A5	09	09
	C3⋈13	10	10
	B2⋈15	11	11
	R3⋈V5	12	12
	M3⋈L5	13	13
	L2⋈J5	14	14
	Q2⋈U5	15	15
A1B12	C1⋈14	I47-00	Normal Input Channels 4-7, Data Bit 00
	C0⋈11	01	01
	T1⋈31	02	02
	N0⋈P4	03	03
	H0⋈E4	04	04
	I1⋈F4	05	05
	S0⋈Z1	06	06
	N1⋈Q4	07	07
	H3⋈E5	08	08
	G2⋈B5	09	09
	C3⋈12	10	10
	B2⋈02	11	11
	R3⋈X5	12	12
	M3⋈05	13	13
	L2⋈M5	14	14
	Q2⋈W5	15	15

All signals are TCS single-ended with signal connector pins designated to the left of the asterisk and unique companion ground connections designated to the right of the asterisk.

Table 7: Normal Channel Interface, Input 0→7

NORMAL OUTPUT CHANNELS 0-7, SET/CLEAR COMMANDS AND DATA INTERFACE

50-PAK LOCATION	CONNECTOR PINS	SIGNAL NAME	FUNCTION
A1A10	W0/51	CLR-00	Clear Normal Output Channel 0
A1B10	W3/53	01	1
A1A10	W3/52	02	2
A1B10	W0/50	03	3
A1A11	W0/51	04	4
A1B11	W3/53	05	5
A1A11	W3/52	06	6
A1B11	W0/50	07	7
A1A10	V0/50	SET-00	Set Normal Output Channel 0
A1B10	U2/35	01	1
A1A10	U2/42	02	2
A1B10	V0/41	03	3
A1A11	V0/50	04	4
A1B11	U2/35	05	5
A1A11	U2/42	06	6
A1B11	V0/41	07	7
A1A10	C1/11	NC0-00	Normal Output Channels 0-7, Data Bit 00
A10	C0/10	⋈NC0-01	Data Bit 01
A10	F0/30	NC0-02	Data Bit 02
A1A10	H1/B4	⋈NC0-03	Data Bit 03
A1A11	C1/11	NC0-04	Data Bit 04
A1A11	C0/10	⋈NC0-05	Data Bit 05
A1A11	F0/30	NC0-06	Data Bit 06
A1A11	H1/B4	⋈NC0-07	Data Bit 07
A1B10	C1/14	NC0-08	Data Bit 08
A1B10	C0/11	⋈NC0-09	Data Bit 09
A1B10	F0/A1	NC0-10	Data Bit 10
A1B10	H1/D4	⋈NC0-11	Data Bit 11
A1B11	C1/14	NC0-12	Data Bit 12
A1B11	C0/11	⋈NC0-13	Data Bit 13
A1B11	F0/A1	NC0-14	Data Bit 14
A1B11	H1/D4	⋈NC0-15	Data Bit 15

All signals are TCS single-ended with the signal connector pins designated to the left of the slash and unique companion ground connections designated to the right of the slash.

Table 7A: Normal Channel Interface, Output 0—7

The following Backpanel inter-connections provide Normal Output Channels 0 → 7 with fan-out for Set and Clear Channel Commands as well as Normal Output Channel Data by daisy-chaining.

Source	Destination	Signal Name
A1A10-W1⋈54	A1B10-G2/B5	CLR-00
A1B10-X2⋈62	A1A10-L2/J5	01
A1A10-X2⋈62	A1B10-L2/M5	02
A1B10-W1⋈51	A1A10-G2/A5	03
A1A11-W1⋈51	A1B11-G2/B5	04
A1B11-X2⋈62	A1A11-L2/J5	05
A1A11-X2⋈62	A1B11-L2/M5	06
A1B11-W1⋈51	A1A11-G2/A5	07
A1A10-U1⋈41	A1B10-F3/A2	SET-00
A1B10-V3⋈42	A1A10-K3/I5	01
A1A10-V3⋈53	A1B10-K3/K5	02
A1B10-U1⋈34	A1A10-F3/33	03
A1A11-U1⋈41	A1B11-F3/A2	04
A1B11-V3⋈42	A1A11-K3/I5	05
A1A11-V3⋈53	A1B11-K3/K5	06
A1B11-U1⋈34	A1A11-F3/33	07
A1A10-D1⋈24	A1A11-N1/N4	NC0-00
A1A10-B0⋈01	A1A11-P1/S4	⋈NC0-01
A1A10-G1⋈A4	A1A11-R1/W4	NC0-02
A1A10-H0⋈C4	A1A11-T0/Z1	⋈NC0-03
A1A11-D1⋈24	A1A10-N1/N4	NC0-04
A1A11-B0⋈01	A1A10-P1/S4	⋈NC0-05
A1A11-G1⋈A4	A1A10-R1/W4	NC0-06
A1A11-H0⋈C4	A1A10-T0/Z1	⋈NC0-07
A1B10-D1⋈24	A1B11-N1/Q4	NC0-08
A1B10-B0⋈00	A1B11-P1/U4	⋈NC0-09
A1B10-G1⋈B4	A1B11-R1/Y4	NC0-10
A1B10-H0⋈E4	A1B11-T0/30	⋈NC0-11
A1B11-D1⋈24	A1B10-N1/Q4	NC0-12
A1B11-B0⋈00	A1B10-P1/U4	⋈NC0-13
A1B11-G1⋈B4	A1B10-R1/Y4	NC0-14
A1B11-H0⋈E4	A1B10-T0/30	⋈NC0-15

Table 7B: Normal Channel Interface, Output 0 → 7, Daisy-Chained

Normal Input Channels 8 → F: Select and Data Interface

50-PAK Location	Connector Pins	Signal Name	Function
A1A07	K0⋈I4	SEL-I8	Select Normal Input Channel 8
↓	M0⋈L4	I9	9
	K1⋈H4	IA	A
	L1⋈J4	IB	B
	D0⋈21	IC	C
	G1⋈A4	ID	D
	J1⋈F4	IE	E
	H1⋈B4	IF	F
A1A02	L0/I4	I8B-00	Normal Input Channels 8-B, Data Bit 00
↓	J1/F4	01	01
	J0/G4	02	02
	G0/A1	03	03
A1B02	L0/L4	04	04
↓	J1/H4	05	05
	J0/I4	06	06
	G0/C4	07	07
A1A09	L0/I4	08	08
↓	J1/F4	09	09
	J0/G4	10	10
	G0/A1	11	11
A1B09	L0/L4	12	12
↓	J1/H4	13	13
	J0/I4	14	14
	G0/C4	15	15
A1A02	M1/M4	ICF-00	Normal Input Channels C-F, Data Bit 00
↓	I0/E4	01	01
	K0/I4	02	02
	H1/B4	03	03
A1B02	M1/N4	04	04
↓	I0/G4	05	05
	K0/K4	06	06
	H1/D4	07	07
A1A09	M1/M4	08	08
↓	I0/E4	09	09
	K0/I4	10	10
	H1/B4	11	11
A1B09	M1/N4	12	12
↓	I0/G4	13	13
	K0/K4	14	14
	H1/D4	15	15

All signals are TCS single-ended with signal connector pins designated to the left of the asterisks/slashes and unique companion ground connections designated to the right of the asterisks/slashes.

Table A: Normal Channel Interface

Normal Output Channels 8→F, Set/Clear Commands and Data Interface

50-PAK Location	Connector Pins	Signal Name	Function
A1A07	X1*61	CLR-08	Clear Normal Output Channel 8
	X0*60	09	9
	W1*54	0A	A
	W0*51	0B	B
	T1*Z4	0C	C
	U0*40	0D	D
	U1*41	0E	E
	V0*50	0F	F
A1A07	Q0*T4	SET-08	Set Normal Output Channel 8
	P1*54	09	9
	P0*R4	0A	A
	01*Q4	0B	B
	R1*W4	0C	C
	S0*X4	0D	D
	S1*Y4	0E	E
	T0*Z1	0F	F
A1A03	J3*G5	*NC0-00	Normal Output Channels 8-F, Data Bit 00
	H2*B5	NC0-01	Data Bit 01
	E3*23	*NC0-02	Data Bit 02
	K3*I5	NC0-03	Data Bit 03
A1B03	J3*I5	*NC0-04	Data Bit 04
	H2*D5	NC0-05	Data Bit 05
	E3*23	*NC0-06	Data Bit 06
	K3*K5	NC0-07	Data Bit 07
A1A08	J2*F5	*NC0-08	Data Bit 08
	F2*32	NC0-09	Data Bit 09
	I3*E5	*NC0-10	Data Bit 10
	I2*D5	NC0-11	Data Bit 11
A1B08	J2*H5	*NC0-12	Data Bit 12
	F2*A5	NC0-13	Data Bit 13
	I3*G5	*NC0-14	Data Bit 14
	I2*F5	NC0-15	Data Bit 15

Table 8A: Normal Channel Interface, Output 8→F

NOTE: All signals are TCS single-ended with the connector pin to the left of the asterisk designated as the signal pin and the companion connection to the right of the asterisk being designated as ground.

Station Control Interface: Pluggable Signals (J01)

Connector Pins	Signal Name	Function
A1/A2	PRS-00	▽P▽ Register Display, Bit 00
A3/A4	01	01
A5/A6	02	02
A7/A8	03	03
A9/A10	04	04
B1/B2	PRS-05	▽P▽ Register Display, Bit 05
B3/B4	06	06
B5/B6	07	07
B7/B8	08	08
B9/B10	09	09
C1/C2	PRS-10	▽P▽ Register Display, Bit 10
C3/C4	11	11
C5/C6	12	12
C7/C8	13	13
C9/C10	14	14
D1/D2	PRS-15	▽P▽ Register Display, Bit 15
D3/D4	JPM-ID	Jump Condition Met Status
D5/D6	RNI-ID	Read Next Instruction Status
D7/D8	RAD-ID	Read Address Status
D9/D10	ROP-ID	Read Operand Status
E1/E2	STO-ID	Store Operand Status
E3/E4	BKP-00	Breakpoint Address, Bit 00
E5/E6	01	01
E7/E8	02	02
E9/E10	03	03
F1/F2	BKP-04	Breakpoint Address, Bit 04
F3/F4	05	05
F5/F6	06	06
F7/F8	07	07

NOTE: All signals are TCS single-ended and are assigned to even-numbered connector pins with the odd-numbered companion pins at ground.

Table 9: Station Control Interface, J01

Station Control Interface: Pluggable Signals {J02}

Connector pins	Signal Name	Function
A1/A2	REG-00	Adder Display, Bit 00
A3/A4	01	01
A5/A6	02	02
A7/A8	03	03
A9/A10	04	04
B1/B2	REG-05	Adder Display, Bit 05
B3/B4	06	06
B5/B6	07	07
B7/B8	08	08
B9/B10	09	09
C1/C2	REG-10	Adder Display, Bit 10
C3/C4	11	11
C5/C6	12	12
C7/C8	13	13
C9/C10	14	14
D1/D2	REG-15	Adder Display, Bit 15
D3/D4	SEL-B1	B1 Register Select
D5/D6	SEL-B2	B2 Register Select
D7/D8	SEL-AR	A Register Select
D9/D10	SEL-SR	S Register Select
E1/E2	ADDOFF	Augend and Addend Not Selected
E3/E4	$\overline{\text{FAST-A}}$	Timing Margins, 1st Half Fast
E5/E6	$\overline{\text{SLOW-A}}$	Timing Margins, 1st Half Slow
E7/E8	$\overline{\text{FAST-B}}$	Timing Margins, 2nd Half Fast
E9/E10	$\overline{\text{SLOW-B}}$	Timing Margins, 2nd Half Slow
F1/F2	SEL-NT	Not "t" Designator Select
F3/F4	SEL-T	"t" Designator Select
F5/F6	SEL-XR	X Register Select
F7/F8	SEL-NX	Not X Register Select

NOTE: All signals are TCS single-ended and are assigned to even-numbered connector pins with the odd-numbered companion pins at ground.

Table 10: Control Interface, J02

Station Control Interface: Pluggable Signals {J03}

Connector Pins	Signal Name	Function
A1/A2	$\overline{\text{SETA00}}$	▽A▽ Register Entry, Bit 00
A3/A4	01	01
A5/A6	02	02
A7/A8	03	03
A9/A10	04	04
B1/B2	$\overline{\text{SETA05}}$	▽A▽ Register Entry, Bit 05
B3/B4	06	06
B5/B6	07	07
B7/B8	08	08
B9/B10	09	09
C1/C2	$\overline{\text{SETA10}}$	▽A▽ Register Entry, Bit 10
C3/C4	11	11
C5/C6	12	12
C7/C8	13	13
C9/C10	14	14
D1/D2	$\overline{\text{SETA15}}$	▽A▽ Register Entry, Bit 15
D3/D4	$\overline{\text{CLR-AR}}$	A Register Clear
D5/D6	$\overline{\text{STOP-S}}$	Stop Switch Input
D7/D8	$\overline{\text{MC-S}}$	Master Clear Switch Input
D9/D10	GO-S	GO Switch Input {N.C.}
E1/E2	$\overline{\text{GO-S}}$	GO Switch Input {N.O.}
E3/E4	$\overline{\text{NOP-OO}}$	Selective Stop Input
E5/E6	$\overline{\text{RUN-ID}}$	NOT Running Status
E7/E8	$\overline{\text{PE-ID}}$	Parity Error
E9/E10	$\overline{\text{EN-PE}}$	Stop on Parity Error Select
F1/F2	$\overline{\text{CLR-PE}}$	Parity Error Clear
F3/F4	$\overline{\text{CLRCHL}}$	Clear Channel
F5/F6	$\overline{\text{SWEEP}}$	Sweep Mode
F7/F8	$\overline{\text{ENTER}}$	Enter Mode

NOTE: All signals are TCS single-ended and are assigned to even-numbered connector pins with the odd-numbered comparion pins at ground.

Table 11: Station Control Interface, J03

Station Control Interface: Pluggable Signals (J04)

Connector Pins	Signal Name	Function
A1/A2	SETP00	▽P▽ Register Entry, Bit 00
A3/A4	01	01
A5/A6	02	02
A7/A8	03	03
A9/A10	04	04
B1/B2	SETP05	▽P▽ Register Entry, Bit 05
B3/B4	06	06
B5/B6	07	07
B7/B8	08	08
B9/B10	09	09
C1/C2	SETP10	▽P▽ Register Entry, Bit 10
C3/C4	11	11
C5/C6	12	12
C7/C8	13	13
C9/C10	14	14
D1/D2	SETP15	▽P▽ Register Entry, Bit 15
D3/D4	CLEARP	P Register Clear
D5/D6	BKP-08	Breakpoint Address, Bit 08
D7/D9	09	09
D9/D10	10	10
E1/E2	BKP-11	Breakpoint Address, Bit 11
E3/E4	12	12
E5/E6	13	13
E7/E8	14	14
E9/E10	15	15
F1/F2	BPI	Breakpoint Instruction Select
F3/F4	BPO	Breakpoint Operand Select
F5/F6	INSTRS	Instruction Step
F7/F8	CYCLES	Cycle Step

NOTE: All signals are TCS single-ended and are assigned to even-numbered connector pins with the odd-numbered companion pins at ground.

Table 12: Station Control Interface, J04

50-PAK Location	Connector Pins	Signal Name	Function
A1B01 ↓	I0/G4 T0/30 K2/J5	$\overline{GO}$ $\overline{STOP}$ $\overline{MC}$	Not GO Not STOP Not Master Clear
A1B01 A1B05 A1B06 A1B01	R2/Y5 D0/10 F3/A2 B3*03	$\overline{DIS-ST}$ $\overline{FORCEF}$ EN-OUT EOP-CC	Enable Storage Write Not Force Function Force Function Select End of Block Transfer Status

NOTE: All signals are TCS single-ended with the connector pin to the left of the slash/asterisk designated as the signal pin and the companion contact to the right of the slash/asterisk designated as ground.

Table 13: Non-Pluggable Station Control Interface

50-PAK Location	Connector Pins	Signal Name	Function
A1A03 ↓	B1*B0 H1*H0 L0*L1 P1*P0	SRM-00 SRM-01 SRM-02 SRM-03	Storage Address, Bit 00 ↓ 01 02 03

NOTE: These signals are TCS differential with the true state level on the connector pin to the left of the asterisk and the negated state on the companion connector pin to the right of the asterisk.

Table 14: Non-Pluggable Storage Interface Signals

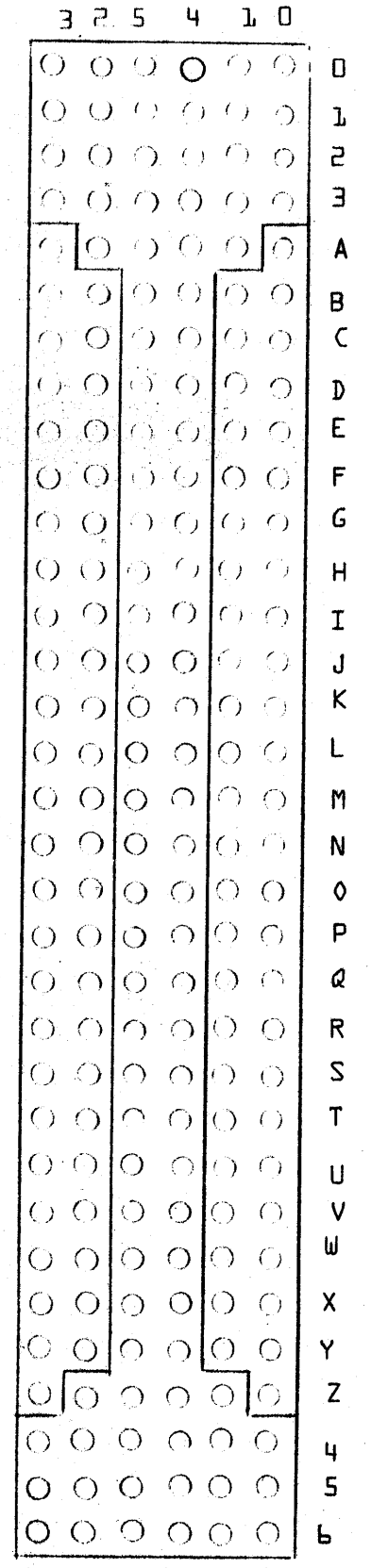
Buffer Controller Backpanel: View from 50-PAK Side

Chassis A1

0	1	2	3	4	5	6	7	8	9	10	11	12	
A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A
B00	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B

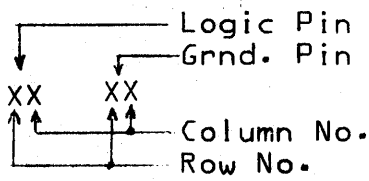
NOTE: For mounting and silk-screen details see Connector Plate, Sub-Assembly: Drawing 52801500 and Connector Plate: Drawing 52762100

Figure 6: Buffer Controller Backpanel



GROUND PIN ASSIGNMENTS

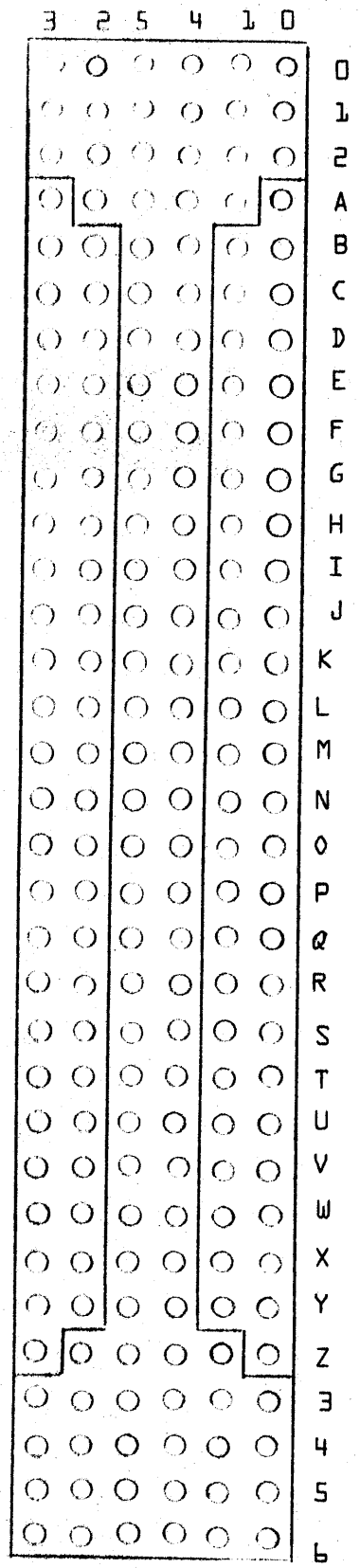
KEY:



A3/03			A0/00
B3/02	B2/15	B1/14	B0/01
C3/13	C2/12	C1/11	C0/10
D3/22	D2/25	D1/24	D0/21
E3/23	E2/35	E1/34	E0/20
F3/33	F2/32	F1/31	F0/30
G3/A2	G2/A5	G1/A4	G0/A1
H3/C5	H2/B5	H1/B4	H0/C4
I3/E5	I2/D5	I1/D4	I0/E4
J3/G5	J2/F5	J1/F4	J0/G4
K3/I5	K2/H5	K1/H4	K0/I4
L3/K5	L2/J5	L1/J4	L0/K4
M3/L5	M2/M5	M1/M4	M0/L4
N3/05	N2/N5	N1/N4	N0/04
03/P5	02/Q5	01/Q4	00/P4
P3/R5	P2/S5	P1/S4	P0/R4
Q3/T5	Q2/U5	Q1/U4	Q0/T4
R3/V5	R2/W5	R1/W4	R0/V4
S3/X5	S2/Y5	S1/Y4	S0/X4
T3/Z2	T2/Z5	T1/Z4	T0/Z1
U3/43	U2/42	U1/41	U0/40
V3/53	V2/45	V1/44	V0/50
W3/52	W2/55	W1/54	W0/51
X3/63	X2/62	X1/61	X0/60
Y3/-	Y2/-	Y1/-	Y0/-
Z3/-			Z0/-

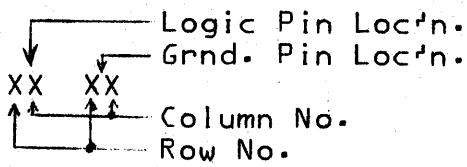
← "A" Row 50-PAK Location
Viewed from the Wiring Side

FIGURE 7: A Row Ground Pin Assignments



GROUND PIN ASSIGNMENTS

KEY:



A3/05			A0/04
B3/03	B2/02	B1/01	B0/00
C3/12	C2/15	C1/14	C0/11
D3/13	D2/25	D1/24	D0/10
E3/23	E2/22	E1/21	E0/20
F3/A2	F2/A5	F1/A4	F0/A1
G3/C5	G2/B5	G1/B4	G0/C4
H3/E5	H2/D5	H1/D4	H0/E4
I3/G5	I2/F5	I1/F4	I0/G4
J3/I5	J2/H5	J1/H4	J0/I4
K3/K5	K2/J5	K1/J4	K0/K4
L3/L5	L2/M5	L1/M4	L0/L4
M3/05	M2/N5	M1/N4	M0/04
N3/P5	N2/Q5	N1/Q4	N0/P4
03/R5	02/S5	01/S4	00/R4
P3/T5	P2/U5	P1/U4	P0/T4
Q3/V5	Q2/W5	Q1/W4	Q0/V4
R3/X5	R2/Y5	R1/Y4	R0/X4
S3/Z2	S2/Z5	S1/Z4	S0/Z1
T3/33	T2/32	T1/31	T0/30
U3/43	U2/35	U1/34	U0/40
V3/42	V2/45	V1/44	V0/41
W3/53	W2/52	W1/51	W0/50
X3/63	X2/62	X1/61	X0/60
Y3/-	Y2/-	Y1/-	Y0/-
Z3/-			Z0/-

← "B" Row 50-PAK Location
Viewed from the wiring side

FIGURE 8 : B Row Ground Pin Assignments

REVISION RECORD

REV.	PAGE	PARAGRAPH	DATA	E.C.O.	APP.	DATE
01			Class B Release			11/5/69